

T-39-13

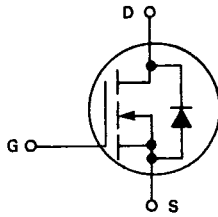
**MOTOROLA SEMICONDUCTOR TECHNICAL DATA**

**IRF840  
IRF841  
IRF842  
IRF843**

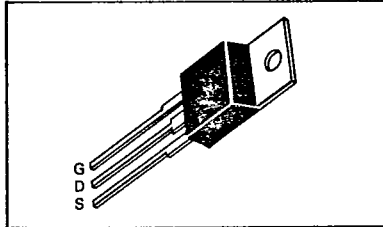
**N-CHANNEL ENHANCEMENT-MODE SILICON GATE  
TMOS POWER FIELD EFFECT TRANSISTOR**

These TMOS Power FETs are designed for high voltage, high speed power switching applications such as switching regulators, converters, solenoid and relay drivers.

- Silicon Gate for Fast Switching Speeds
- Low  $r_{DS(on)}$  to Minimize On-Losses. Specified at Elevated Temperature
- Rugged — SOA is Power Dissipation Limited
- Source-to-Drain Diode Characterized for Use With Inductive Loads



Part Number	$V_{DSS}$	$r_{DS(on)}$	$I_D$
IRF840	500 V	0.85 $\Omega$	8.0 A
IRF841	450 V	0.85 $\Omega$	8.0 A
IRF842	500 V	1.10 $\Omega$	7.0 A
IRF843	450 V	1.10 $\Omega$	7.0 A



**MAXIMUM RATINGS**

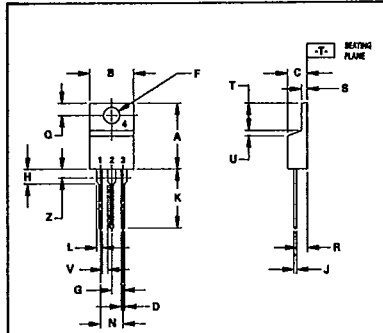
Rating	Symbol	IRF				Unit
		840	841	842	843	
Drain-Source Voltage	$V_{DSS}$	500	450	500	450	Vdc
Drain-Gate Voltage ( $R_{GS} = 1.0 \text{ m}\Omega$ )	$V_{DGR}$	500	450	500	450	Vdc
Gate-Source Voltage	$V_{GS}$	$\pm 20$				Vdc
Drain Current Continuous Pulsed	$I_D$	8.0		7.0		Acd
	$I_{DM}$	32		28		
Total Power Dissipation @ $T_C = 25^\circ\text{C}$ Derate above $25^\circ\text{C}$	$P_D$	125 1.0				Watts W/°C
Operating and Storage Temperature Range	$T_J, T_{stg}$	-55 to 150				°C

**THERMAL CHARACTERISTICS**

Thermal Resistance Junction to Case Junction to Ambient	$R_{\theta JC}$	1.0	°C/W
	$R_{\theta JA}$	62.5	
Maximum Lead Temp. for Soldering Purposes, 1/8" from Case for 5 Seconds	$T_L$	275	°C

See the MTP8N45 Designer's Data Sheet for a complete set of design curves for the product on this data sheet.

The Designer's Data Sheet permits the design of most circuits entirely from the information presented. Limit curves — representing boundaries on device characteristics — are given to facilitate "worst case" design.



STYLE 5  
PIN 1, GATE  
2, DRAIN  
3, SOURCE  
4, DRAIN

- NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSIS Y14.5M, 1982
  2. CONTROLLING DIMENSION, INCH
  3. DIM Z DEFINES A ZONE WHERE ALL BODY AND LEAD IRREGULARITIES ARE ALLOWED

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	14.48	15.75	0.570	0.620
B	9.68	12.28	0.380	0.485
C	4.07	4.82	0.160	0.190
D	0.84	0.98	0.033	0.039
F	3.61	3.73	0.142	0.147
G	2.42	2.66	0.095	0.106
H	2.80	2.93	0.110	0.116
J	0.96	0.95	0.038	0.037
K	12.70	14.27	0.500	0.562
L	1.15	1.29	0.045	0.051
N	4.83	5.33	0.190	0.210
O	2.54	3.04	0.100	0.120
A	2.04	2.79	0.080	0.110
S	1.15	1.29	0.045	0.051
T	5.97	6.47	0.235	0.255
U	0.00	1.27	0.000	0.050
V	1.15	—	0.045	—
Z	—	2.54	—	0.000

CASE 221A-04  
TO-220AB

**ELECTRICAL CHARACTERISTICS** (T<sub>C</sub> = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit	
<b>OFF CHARACTERISTICS</b>					
Drain-Source Breakdown Voltage (V <sub>GS</sub> = 0, I <sub>D</sub> = 0.25 mA)	IRF841, IRF843 IRF840, IRF842	V <sub>(BR)DSS</sub>	450 500	— —	Vdc
Zero Gate Voltage Drain Current (V <sub>DS</sub> = Rated V <sub>DSS</sub> , V <sub>GS</sub> = 0) (V <sub>DS</sub> = 0.8 Rated V <sub>DSS</sub> , V <sub>GS</sub> = 0, T <sub>J</sub> = 125°C)		I <sub>DSS</sub>	— —	0.25 1.00	mAdc
Gate-Body Leakage Current, Forward (V <sub>GSF</sub> = 20 Vdc, V <sub>DS</sub> = 0)		I <sub>GSSF</sub>	—	500	nAdc
Gate-Body Leakage Current, Reverse (V <sub>GSR</sub> = 20 Vdc, V <sub>DS</sub> = 0)		I <sub>GSSR</sub>	—	500	nAdc
<b>ON CHARACTERISTICS*</b>					
Gate Threshold Voltage (V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = 0.25 mA)		V <sub>GS(th)</sub>	2.0	4.0	Vdc
Static Drain-Source On-Resistance (V <sub>GS</sub> = 10 Vdc, I <sub>D</sub> = 4.0 Adc)	IRF840, IRF841 IRF842, IRF843	r <sub>DS(on)</sub>	— —	0.85 1.0	Ohm
On-State Drain Current (V <sub>GS</sub> = 10 V) (V <sub>DS</sub> ≥ 6.8 Vdc) (V <sub>DS</sub> ≥ 7.0 Vdc)	IRF840, IRF841 IRF842, IRF843	I <sub>D(on)</sub>	8.0 7.0	— —	Adc
Forward Transconductance (V <sub>DS</sub> ≥ 6.8 V, I <sub>D</sub> = 4.0 A) (V <sub>DS</sub> ≥ 7.0 V, I <sub>D</sub> = 4.0 A)	IRF840, IRF841 IRF842, IRF843	g <sub>FS</sub>	4.0 4.0	— —	mhos
<b>DYNAMIC CHARACTERISTICS</b>					
Input Capacitance	(V <sub>DS</sub> = 25 V, V <sub>GS</sub> = 0, f = 1.0 MHz)	C <sub>iss</sub>	—	1600	pF
Output Capacitance		C <sub>oss</sub>	—	350	
Reverse Transfer Capacitance		C <sub>rss</sub>	—	150	
<b>SWITCHING CHARACTERISTICS*</b>					
Turn-On Delay Time	(V <sub>DD</sub> ≈ 200 V, I <sub>D</sub> = 4.0 Apk, R <sub>gen</sub> = 4.7 Ohms)	t <sub>d(on)</sub>	—	35	ns
Rise Time		t <sub>r</sub>	—	15	
Turn-Off Delay Time		t <sub>d(off)</sub>	—	90	
Fall Time		t <sub>f</sub>	—	30	
Total Gate Charge	(V <sub>GS</sub> = 10 V, V <sub>DS</sub> = 0.8 × Rated V <sub>DSS</sub> , I <sub>D</sub> = Rated I <sub>D</sub> )	Q <sub>g</sub>	40 (Typ)	60	nC
Gate-Source Charge		Q <sub>gs</sub>	20 (Typ)	—	
Gate-Drain Charge		Q <sub>gd</sub>	20 (Typ)	—	
<b>SOURCE DRAIN DIODE CHARACTERISTICS*</b>					
Forward On-Voltage	(I <sub>S</sub> = Rated I <sub>D</sub> , V <sub>GS</sub> = 0)	V <sub>SD</sub>	—	1.9 (1)	Vdc
Forward Turn-On Time		t <sub>on</sub>	Limited by stray inductance		
Reverse Recovery Time		t <sub>rr</sub>	600 (Typ)	—	ns
<b>INTERNAL PACKAGE INDUCTANCE (TO-220)</b>					
Internal Drain Inductance (Measured from the contact screw on tab to center of die) (Measured from the drain lead 0.25" from package to center of die)	L <sub>d</sub>	3.5 (Typ) 4.5 (Typ)	— —	—	nH
Internal Source Inductance (Measured from the source lead 0.25" from package to source bond pad)	L <sub>s</sub>	7.5 (Typ)	—	—	

\*Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2.0%.  
 (1) Add 0.1 V for IRF840 and IRF841.