

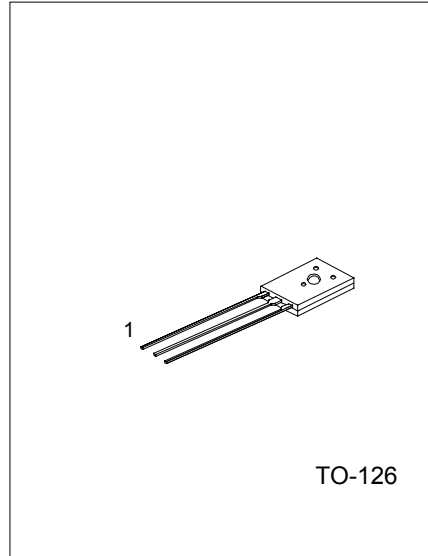
# UTC MJE13002 NPN EPITAXIAL SILICON TRANSISTOR

## NPN SILICON POWER TRANSISTOR

The UTC MJE13002 designed for use in high-voltage, high speed, power switching in inductive circuit. It is particularly suited for 115 and 220V switchmode applications such as switching regulator's, inverters, DC-DC converter, Motor control, Solenoid/Relay drivers and deflection circuits.

### FEATURES

- \*Collector-Emitter Sustaining Voltage:  
V<sub>CEO (sus)</sub>=300V.
- \*Collector-Emitter Saturation Voltage:  
V<sub>CE(sat)</sub>=1.0V(Max.) @I<sub>C</sub>=1.0A, I<sub>B</sub> =0.25A
- \*Switch Time- t<sub>r</sub> =0.7 μs(Max.) @I<sub>C</sub>=1.0A.



1: BASE 2:COLLECTOR 3: EMITTER

### ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	RATING	UNIT
Collector-Emitter Voltage	V <sub>CEO (sus)</sub>	300	V
Collector-Emitter Voltage	V <sub>CEV</sub>	600	V
Emitter Base Voltage	V <sub>EBO</sub>	9	V
Collector Current - Continuous	I <sub>C</sub>	1.5	A
- Peak (1)	I <sub>CM</sub>	3	
Base Current - Continuous	I <sub>B</sub>	0.75	A
- Peak (1)	I <sub>BM</sub>	1.5	
Emitter Current - Continuous	I <sub>E</sub>	2.25	A
- Peak (1)	I <sub>EM</sub>	4.5	
Total Power Dissipation @ TA=25°C	P <sub>D</sub>	1.4	Watts
Derate above 25°C		11.2	MW/°C
Total Power Dissipation @ TC=25°C	P <sub>D</sub>	40	Watts
Derate above 25°C		320	MW/°C
Operating and Storage Junction Temperature Range	T <sub>j</sub> , T <sub>stg</sub>	-65 to +150	°C

### THERMAL CHARACTERISTICS

CHARACTERISTIC	SYMBOL	MAX	UNIT
Thermal Resistance, Junction to Case	R <sub>θ JC</sub>	3.12	°C/W
Thermal Resistance, Junction to Ambient	R <sub>θ JA</sub>	89	°C/W
Maximum Load Temperature for Soldering Purposes: 1/8" from Case for 5 Seconds	T <sub>L</sub>	275	°C

(1) Pulse Test : Pulse Width=5ms, Duty Cycle ≤10%

# UTC MJE13002 NPN EPITAXIAL SILICON TRANSISTOR

Designer's Data for "Worst Case" Conditions – The Designer's Data Sheet permits the design of most circuits entirely from the information presented. SOA Limit curves – representing boundaries on device characteristics – are given to facilitate "Worst case" design.

## ELECTRICAL CHARACTERISTICS (Tc=25°C unless otherwise noted)

CHARACTERISTIC	SYMBOL	MIN	TYP	MAX	UNIT
<b>OFF CHARACTERISTICS (1)</b>					
Collector-Emitter Sustaining Voltage (Ic=10 mA, IB=0)	VCE(SUS)	300			V
Collector Cutoff Current (VCEV=Rated Value, VBE(off)=1.5 V) (VCEV=Rated Value, VBE(off)=1.5V, Tc=100°C)	ICEV			1 5	mA
Emitter Cutoff Current (VEB=9 V, Ic=0)	IEBO			1	mA
<b>SECOND BREAKDOWN</b>					
Second Breakdown Collector Current with base forward biased	Is/b		See Figure 10		
Clamped Inductive SOA with base reverse biased	RBSOA		See Figure 11		
<b>ON CHARACTERISTICS (1)</b>					
DC Current Gain (Ic=0.5 A, VCE=2 V) (Ic=1 A, VCE=2 V)	hFE1 hFE2	8 5		40 25	
Collector-Emitter Saturation Voltage (Ic=0.5A, IB=0.1A) (Ic=1A, IB=0.25A) (Ic=1.5A, IB=0.5A) (Ic=1A, IB=0.25A, Tc=100°C)	VCE(sat)			0.5 1 3 1	V
Base-Emitter Saturation Voltage (Ic=0.5A, IB=0.1A) (Ic=1A, IB=0.25 A) (Ic=1A, IB=0.25A, Tc=100°C)	VBE(sat)			1 1.2 1.1	V
<b>DYNAMIC CHARACTERISTICS</b>					
Current-Gain-Bandwidth Product (Ic=100mA, VCE=10 V, f=1MHz)	fT	4	10		MHz
Output Capacitance (VCB=10V, IE=0, f=0.1MHz)	Cob		21		pF
<b>SWITCHING CHARACTERISTICS(TABLE 1)</b>					
Delay Time	td		0.05	0.1	μs
Rise Time	tr	(Vcc=125V, Ic=1A, IB1=IB2=0.2A, tp=25 μs, Duty Cycle≤1%)	0.5	1	μs
Storage Time	ts		2	4	μs
Fall Time	tf		0.4	0.7	μs
<b>INDUCTIVE LOAD, CLAMPED (TABLE 1,FIGURE 12)</b>					
Storage Time	tsv		1.7	4	μs
Crossover Time	tc	(Ic=1A, Vclamp=300V, IB1=0.2A, VBE(off)=5V, Tc=100°C)	0.29	0.75	μs
Fall Time	tft		0.15		μs

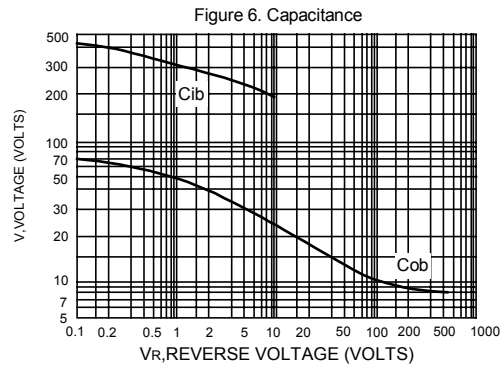
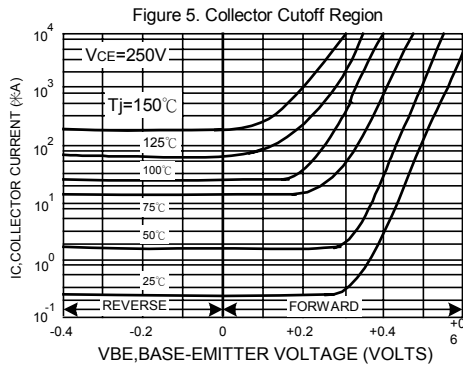
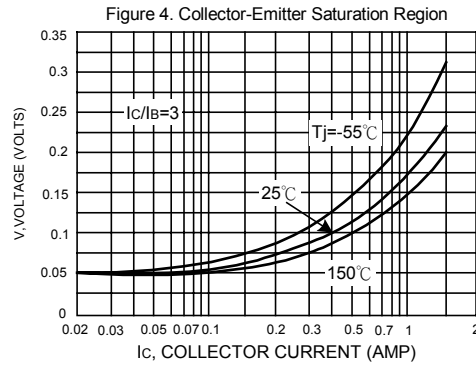
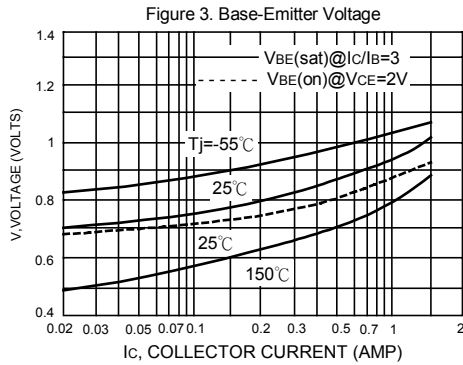
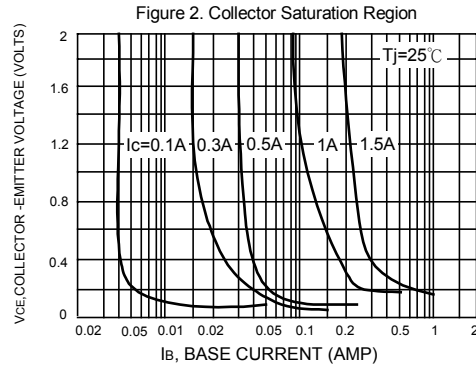
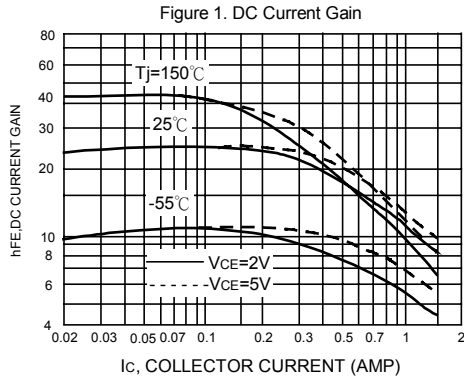
(1) Pulse Test : PW=300 μs, Duty Cycle≤2%

## CLASSIFICATION OF HFE1

RANK	A	B	C	D	E	F
RANGE	8 ~ 16	15 ~ 21	20 ~ 26	25 ~ 31	30 ~ 36	35 ~ 40

# UTC MJE13002 NPN EPITAXIAL SILICON TRANSISTOR

## TYPICAL PERFORMANCE CHARACTERISTICS



# UTC MJE13002 NPN EPITAXIAL SILICON TRANSISTOR

TABLE 1. TEST CONDITIONS FOR DYNAMIC PERFORMANCE

REVERSE BIAS SAFE OPERATING AREA AND INDUCTIVE SWITCHING			RESISTIVE SWITCHING
TEST CIRCUITS	<p>NOTE PW and Vcc Adjusted for Desired Ic RB Adjusted for Desired IB1</p>		
CIRCUIT VALUES	<p>Coil Data : FERROXCUBE core #6656 Full Bobbin (-200 Turns) #20</p> <p>GAP for 30 mH/2 A Lcoil=50mH</p> <p>Vcc=20V Vclamp=300V</p>		<p>Vcc=125V Rc=125 Ω D1=1N5820 or Equiv. RB=47 Ω</p>
TEST WAVEFORMS	<p>OUTPUT WAVEFORMS</p> <p><math>t_1</math> Adjusted to Obtain Ic</p> $t_1 = \frac{L_{coil}(I_{c(pk)})}{V_{cc}}$ $t_2 = \frac{L_{coil}(I_{c(pk)})}{V_{clamp}}$ <p>Test Equipment Scope-Tektronics 475 or Equivalent</p>		<p><math>t_r, t_f &lt; 10ns</math> Duty Cycle=1.0% Rb and Rc adjusted for desired Ib and Ic</p>

TABLE 2. TYPICAL INDUCTIVE SWITCHING PERFORMANCE

Ic AMP	Tc °C	Tsv μ s	Trv μ s	Tfi μ s	Tti μ s	Tc μ s
0.5	25	1.3	0.23	0.30	0.35	0.30
	100	1.6	0.26	0.30	0.40	0.36
1	25	1.5	0.10	0.14	0.05	0.16
	100	1.7	0.13	0.26	0.06	0.29
1.5	25	1.8	0.07	0.10	0.05	0.16
	100	3	0.08	0.22	0.08	0.28

Note: All Data Recorded in the inductive Switching Circuit Table 1

# UTC MJE13002 NPN EPITAXIAL SILICON TRANSISTOR

---

## SWITCHING TIMES NOTE

In resistive switching circuits, rise, fall, and storage times have been defined and apply to both current and voltage waveforms since they are in phase. However, for inductive loads which are common to SWITCHMODE power supplies and hammer drivers, current and voltage waveforms are not in phase. Therefore, separate measurements must be made on each wave form to determine the total switching time. For this reason, the following new terms have been defined.

tsv=Voltage Storage Time, 90%  $I_{B1}$  to 10%  $V_{clamp}$

trv=Voltage Rise Time, 10-90%  $V_{clamp}$

tff=Current Fall Time, 90-10%  $I_c$

ttr=Current Tail, 10-2%  $I_c$

tc=Crossover Time, 10%  $V_{clamp}$  to 10%  $I_C$

An enlarged portion of the inductive switching waveforms is shown in Figure 7 to aid in the visual identity of these terms.

For the designer, there is minimal switching loss during storage time and the predominant switching power losses occur during the crossover interval and can be obtained using the standard equation from AN-222:

$$PSWT = 1/2 V_{cc} (t_c) f$$

In general,  $trv + tff \approx tc$ . However, at lower test currents this relationship may not be valid.

As is common with most switching transistor, resistive switching is specified at 25°C and has become a benchmark for designers. However, for designers of high frequency converter circuits, the user oriented specifications which make this a "SWITCHMODE" transistor are the inductive switching speeds ( $t_c$  and  $tsv$ ) which are guaranteed at 100°C

## SAFE OPERATING AREA INFORMATION

### FORWARD BIAS

There are two limitations on the power handling ability of a transistor: average junction temperature and second break-down. Safe operating area curves indicate  $I_c - V_{CE}$  limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 10 is based on  $T_c = 25^\circ\text{C}$ ;  $T_J(pk)$  is variable depending on power level. Second breakdown pulse limits are valid for duty cycles to 10% but must be derated when  $T_c \geq 25^\circ\text{C}$ . Second breakdown limitations do not derate the same as thermal limitations. Allowable current at the voltages shown on Figure 10 may be found at any case temperature by using the appropriate curve on Figure 12.

$T_J(pk)$  may be calculated from the data in Figure 10. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

### REVERSE BIAS

For inductive loads, high voltage and high current must be sustained simultaneously during turn-off, in most cases, with the base to emitter junction reverse biased. Under these conditions the collector voltage must be held to a safe level at or below a specific value of collector current. This can be accomplished by several means such as active clamping, RC snubbing, load line shaping, etc. The safe level for these devices is specified as Reverse Bias Safe Operating Area and represents the voltage-current conditions during re-verse biased turn-off. This rating is verified under clamped conditions so that the device is never subjected to an avalanche mode. Figure 11 gives RBSOA characteristics.

# UTC MJE13002 NPN EPITAXIAL SILICON TRANSISTOR

Figure 7. Inductive Switching Measurements

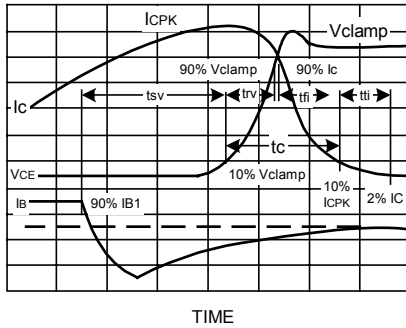


Figure 8. Turn-On Time

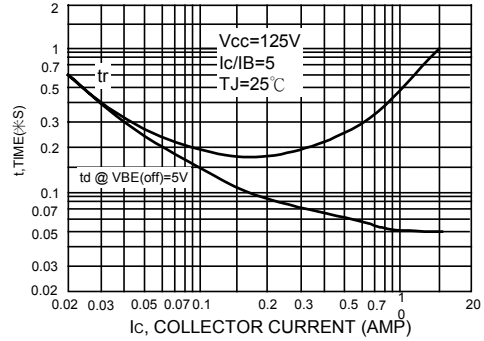


Figure 9. Turn-Off Time

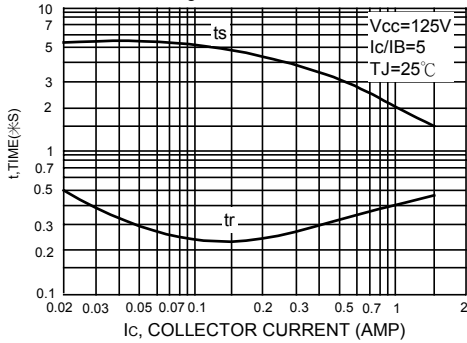


Figure 10. Active Region Safe Operating Area

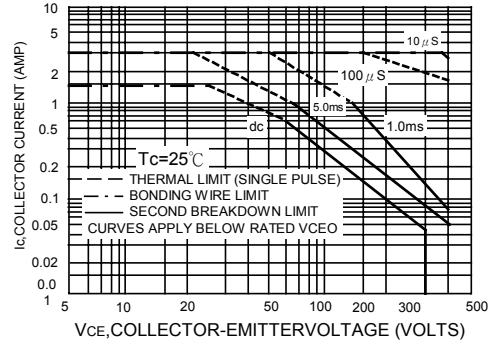


Figure 11. Reverse Bias Safe Operating Area

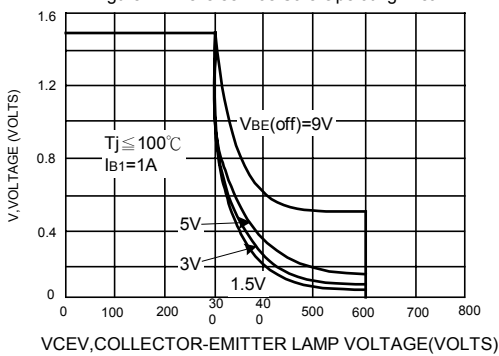
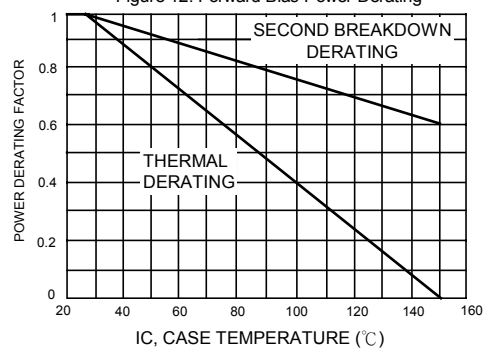
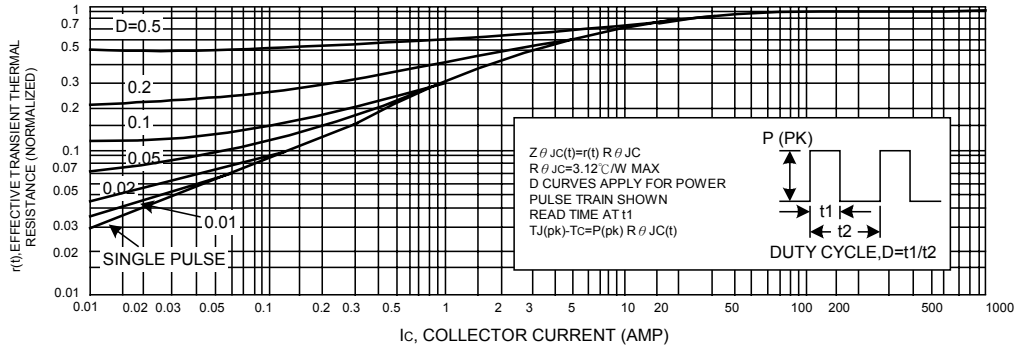


Figure 12. Forward Bias Power Derating



# UTC MJE13002 NPN EPITAXIAL SILICON TRANSISTOR

Figure 13. Thermal Response



UTC assumes no responsibility for equipment failures that result from using products at values that exceed, even momentarily, rated values (such as maximum ratings, operating condition ranges, or other parameters) listed in products specifications of any and all UTC products described or contained herein. UTC products are not designed for use in life support appliances, devices or systems where malfunction of these products can be reasonably expected to result in personal injury. Reproduction in whole or in part is prohibited without the prior written consent of the copyright owner. The information presented in this document does not form part of any quotation or contract, is believed to be accurate and reliable and may be changed without notice.