36V Low Power Dual/Quad Differential Comparators

Features

- Wide Single-supply Voltage Range or Dual Supplies: +2 V to +36 V or ±1.0 V to ±18 V
- Very Low Supply Current (150 μA/ch) Independent of Supply Voltage(0.75 mW/comparator at +5 V)
- Low Input Bias Current：4 nA typ.
- Low Offset Voltage： ± 3.0 mV Max
- Input Common-mode Voltage Range Includes Ground
- Internal Differential Input Voltage Range Equal to The Supply Voltage
- TTL, DTL, ECL, MOS, CMOS compatible Outputs
- ESD Clamps on the Inputs Increase the Ruggedness of the Device Without Affecting Performance
- Low Output Saturation
- –40°C to 125°C Operation Range
- ESD Rating：
  Robust 2KV – HBM, 1KV – CDM
- High Performance Drop-In Compatible With 339, 339, 2903, 2901 Series Product

Applications

- High-speed Line or Digital Line Receivers
- High Speed Sampling Circuits
- Peak and Zero-crossing Detectors
- Threshold Detectors/Discriminators
- Sensing at Ground or Supply Line

Description

The devices in this series consist of dual/quad independent single or dual supply voltage comparators on a single monolithic substrate. The common mode input voltage range includes ground even when operated from a single supply, and the low power supply current drain makes these comparators suitable for battery operation. These types were designed to directly interface with TTL and CMOS, Current drain is independent of the supply voltage. The outputs can be connected to other open-collector outputs to achieve wired-AND relationships.

The LM393 is dual channel version available in 8-pin SOP package. The LM339 is quad channel version available in 14-pin SOP package. All devices are specified for the temperature range of –40°C to +125°C.

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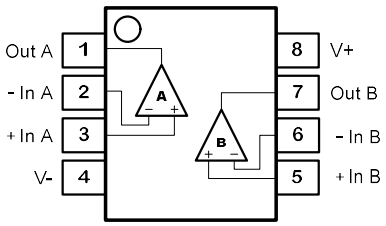
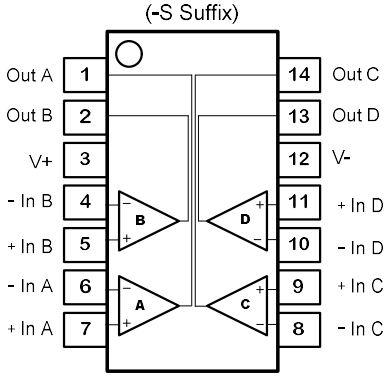
Pin Configuration (Top View)

LM393
8-Pin SOIC
(-S Suffix)



LM339
14-Pin SOIC
(-S Suffix)



Order Information

Model Name	Order Number	Package	Transport Media, Quantity	Marking Information
LM393	LM393-SR	8-Pin SOP	Tape and Reel, 4,000	LM393
LM339	LM339-SR	14-Pin SOP	Tape and Reel, 2,500	LM339
LM339	LM339-TR	14-Pin TSSOP	Tape and Reel, 3,000	LM339

Absolute Maximum Ratings Note 1

Supply Voltage: $V^+ – V^-$.....42V
Input Voltage..... V^- – 0.3 to V^+ + 0.3
Input Current: +IN, –IN, Note 2.....±20mA
Output Current: OUT..... ±20mA
Output Short-Circuit Duration Note 3..... Infinite

Operating Temperature Range.....–40°C to 125°C
Maximum Junction Temperature..... 150°C
Storage Temperature Range..... –65°C to 150°C
Lead Temperature (Soldering, 10 sec) ..... 260°C

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: The inputs are protected by ESD protection diodes to each power supply. If the input extends more than 500mV beyond the power supply, the input current should be limited to less than 10mA.

Note 3: A heat sink may be required to keep the junction temperature below the absolute maximum. This depends on the power supply voltage and how many amplifiers are shorted. Thermal resistance varies with the amount of PC board metal connected to the package. The specified values are for short traces connected to the leads.

ESD, Electrostatic Discharge Protection

Symbol	Parameter	Condition	Minimum Level	Unit
HBM	Human Body Model ESD	ANSI/ESDA/JEDEC JS-001	2	kV
CDM	Charged Device Model ESD	ANSI/ESDA/JEDEC JS-002	1	kV

Thermal Information

Package	$R_{\Theta JA}$	$R_{\Theta JC(Top)}$	Unit
8-Pin SOP	112.4	64.1	°C/W
14-Pin SOP	96.7	46.7	°C/W
14-Pin TSSOP	108.1	42.7	°C/W

Electrical Characteristics

The ● denotes the specifications which apply over the full operating temperature range(-40°C ~ +125°C), otherwise specifications are at T_A = 27°C. V_{DD} = +5V, V_{IN+} = V_{DD}, V_{IN-} = 1.2V, R_{PU}=10kΩ, C_L =15pF.

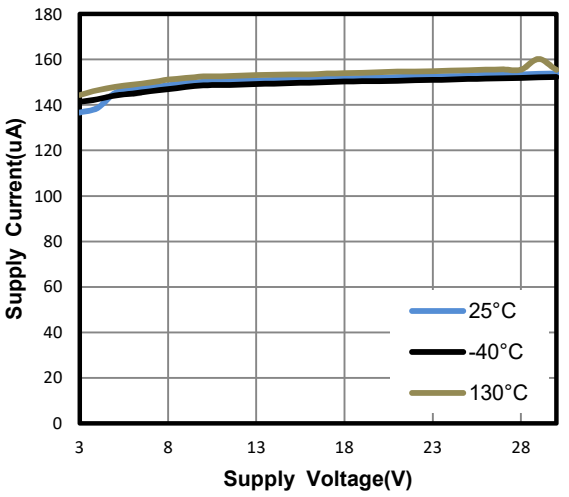
SYMBOL	PARAMETER	CONDITIONS			MIN	TYP	MAX	UNITS
V_{DD}	Supply Voltage			●	2		36	V
V_{OS}	Input Offset Voltage Note 1	V_{CC} = 5 V to MAX, V_{IC} = V_{ICR}(min), V_O = 1.4V			-3	±0.6	+3	mV
V_{OS} TC	Input Offset Voltage Drift Note 1	V_{CM} = 1.2V				1		μV/°C
I_B	Input Bias Current	V_{DM} = 0.5V				4		nA
I_{os}	Input offset Current	V_{DM} = 0.5V				1		nA
C_{IN}	Input Capacitance	Differential Common Mode				2.5 5		pF
V_{CM}	Common-mode Input Voltage Range	25°C			0		V_{DD}-1.5	V
		-40°C ~ +125°C		●	0		V_{DD}-2	V
A_{VD}	Large-signal Differential-voltage Amplification	V_{CC} = 15 V, V_O = 1.4 V to 11.4 V, R_L ≥ 15 kΩ to V_{CC}				100		V/mV
I_{OH}	High-level Output Current	V_{OH} = 5 V, V_{ID} = 1 V				25	70	nA
		V_{OH} = 30 V, V_{ID} = 1 V					7	μA
V_{OL}	Low-Level Output Voltage	I_{OL} = 4mA, V_{ID} = −1V				250	400	mV
				●			700	mV
I_{OL}	Low-level Output Current	V_{OL} = 1.5 V, V_{ID} = −1 V			10			mA
I_Q	Quiescent Current per Comparator	V_{CC} = 5 V				140	290	μA
		V_{CC} = 30 V				150	300	μA
t_{RT}	Response time	R_L connected to 5 V through 5.1 kΩ, C_L = 15 pF, See Note 3	100-mV input step with 5-mV overdrive			2		μs
			TTL-level input step			0.5		

Note 1: The input offset voltage is the average of the input-referred trip points.

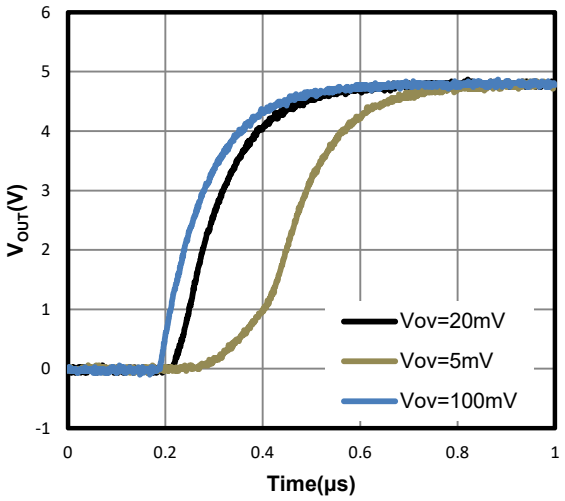
Typical Performance Characteristics

V_S = +5V, V_{CM} = 0V, R_L = Open, unless otherwise specified.

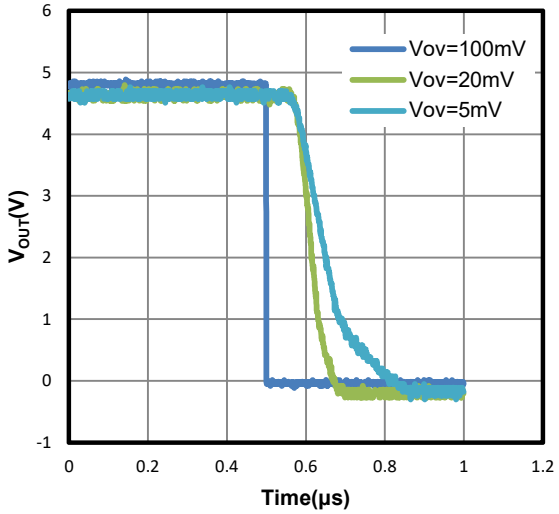
Supply Current vs. Supply Voltage



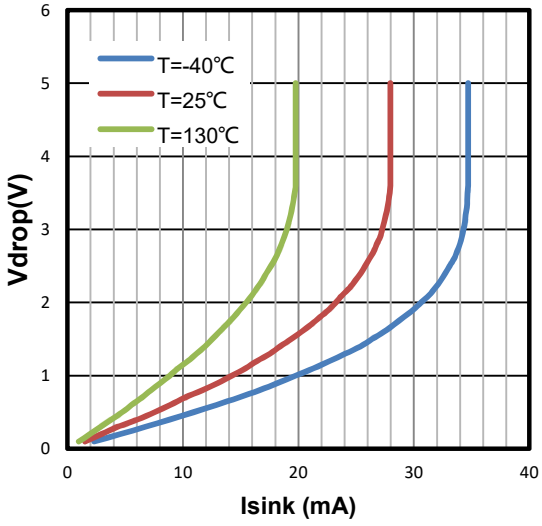
Response Time for Various Input Overdrives – Positive Transition

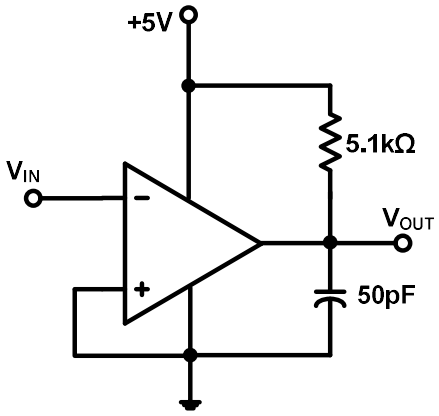


Response Time For Various Input Overdrives - Negative Transition



Negative Output Swing vs. Sink Current





Response Time Test Circuit

Pin Functions

–IN: Inverting Input of the Comparator. Voltage range of this pin can go from V^- to V^+ - 1.5V.
+IN: Non-Inverting Input of Comparator. This pin has the same voltage range as –IN.
V+ (V_{DD}): Positive Power Supply. Typically the voltage is from 2V to 36V. Split supplies are possible as long as the voltage between V+ and V– is between 2V and 36V. A bypass capacitor of 0.1μF as close to the part as possible should be used between power supply pins or between supply pins and ground.
V– (V_{SS}): Negative Power Supply. It is normally tied to ground. It can also be tied to a voltage other than ground as long as the voltage between V^+ and V^- is from 2V to 36V. If it is not connected to ground, bypass it with a capacitor of 0.1μF as close to the part as possible.
OUT: Comparator Output. The voltage range extends to within millivolts of each supply rail.

Operation

The LM393/339 family single-supply comparators feature internal hysteresis, high speed, and low power. Input signal range extends beyond the negative and positive power supplies. The output can even extend all the way to the negative supply. The input stage is active over different ranges of common mode input voltage. Rail-to-rail input voltage range and low-voltage single-supply operation make these devices ideal for portable equipment.

Applications Information

Inputs

The LM393/339 comparator family uses CMOS transistors at the input which prevent phase inversion when the input pins exceed the supply voltages. Figure 1 shows an input voltage exceeding both supplies with no resulting phase inversion.

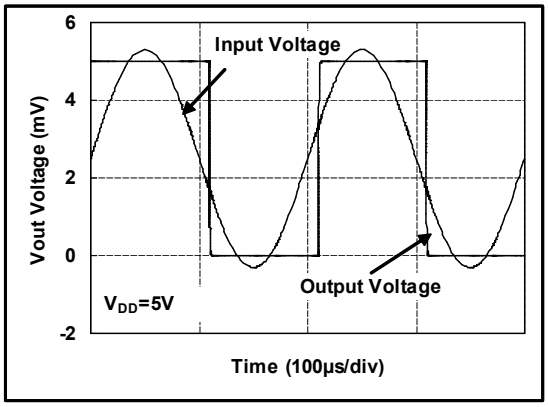


Figure 1. Comparator Response to Input Voltage

The electrostatic discharge (ESD) protection input structure of two back-to-back diodes and 1kΩ series resistors are used to limit the differential input voltage applied to the precision input of the comparator by clamping input voltages that exceed supply voltages, as shown in Figure **2**. Large differential voltages exceeding the supply voltage should be avoided to prevent damage to the input stage.

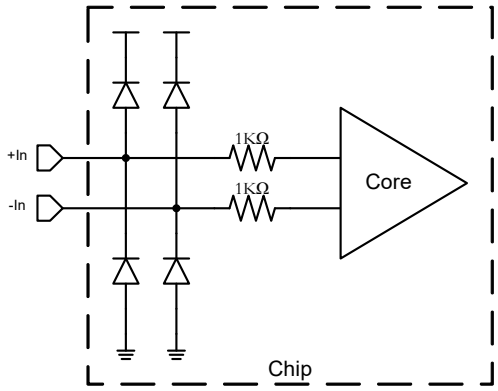


Figure 2. Equivalent Input Structure

External Hysteresis

Greater flexibility in selecting hysteresis is achieved by using external resistors. Hysteresis reduces output chattering when one input is slowly moving past the other. It also helps in systems where it is best not to cycle between high and low states too frequently (e.g., air conditioner thermostatic control). Output chatter also increases the dynamic supply current.

Non-Inverting Comparator with Hysteresis

A non-inverting comparator with hysteresis requires a two-resistor network, as shown in Figure 3 and a voltage reference (V_r) at the inverting input.

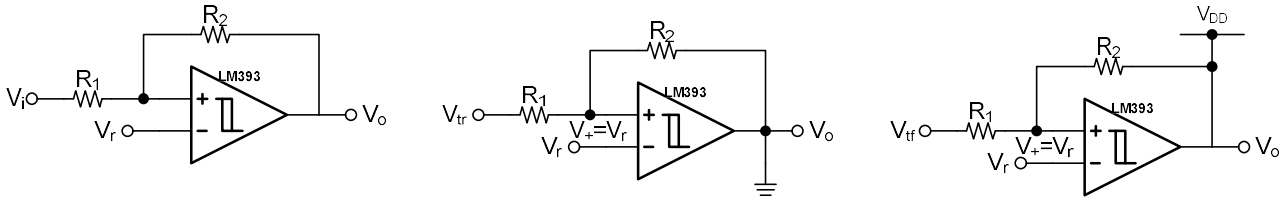


Figure 3. Non-Inverting Configuration with Hysteresis

When Vi is low, the output is also low. For the output to switch from low to high, Vi must rise up to Vtr. When Vi is high, the output is also high. In order for the comparator to switch back to a low state, Vi must equal Vtf before the non-inverting input V+ is again equal to Vr.

$$V_r = \frac{R_2}{R_1 + R_2} V_{tr}$$

$$V_r = (V_{DD} - V_{tf}) \frac{R_1}{R_1 + R_2} + V_{tf}$$

$$V_{tr} = \frac{R_1 + R_2}{R_2} V_r$$

$$V_{tf} = \frac{R_1 + R_2}{R_2} V_r - \frac{R_1}{R_2} V_{DD}$$

$$V_{hyst} = V_{tr} - V_{tf} = \frac{R_1}{R_2} V_{DD}$$

Inverting Comparator with Hysteresis

The inverting comparator with hysteresis requires a three-resistor network that is referenced to the comparator supply voltage (VDD), as shown in Figure 4.

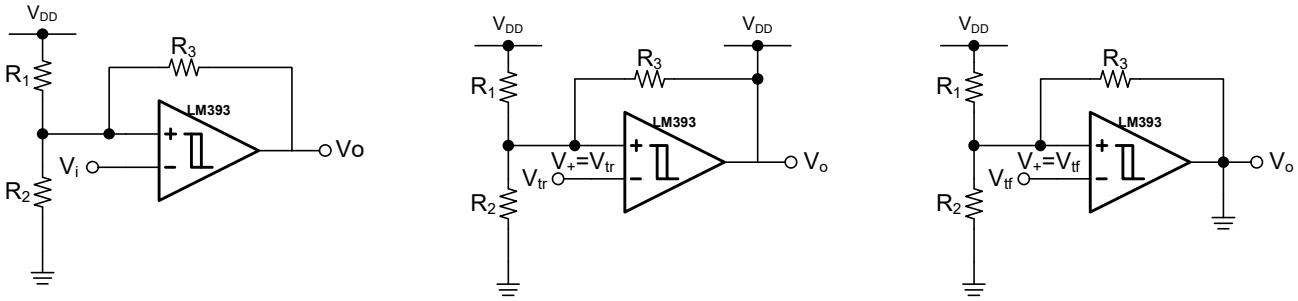


Figure 4. Inverting Configuration with Hysteresis

When Vi is greater than V+, the output voltage is low. In this case, the three network resistors can be presented as paralleled resistor R2 || R3 in series with R1. When Vi at the inverting input is less than V+, the output voltage is high. The three network resistors can be represented as R1 ||R3 in series with R2.

$$V_{tr} = \frac{R_2}{R_1 \parallel R_3 + R_2} V_{DD}$$

$$V_{tf} = \frac{R_2 \parallel R_3}{R_2 \parallel R_3 + R_1} V_{DD}$$

$$V_{hyst} = V_{tr} - V_{tf} = \frac{R_1 \parallel R_2}{R_1 \parallel R_2 + R_3} V_{DD}$$

Low Input Bias Current

The LM393/339 family is a CMOS comparator family and features very low input bias current in pA range. The low input bias current allows the comparators to be used in applications with high resistance sources. Care must be taken to minimize PCB Surface Leakage. See below section on “PCB Surface Leakage” for more details.

PCB Surface Leakage

In applications where low input bias current is critical, Printed Circuit Board (PCB) surface leakage effects need to be considered. Surface leakage is caused by humidity, dust or other contamination on the board. Under low humidity conditions, a typical resistance between nearby traces is $10^{12}\Omega$. A 5V difference would cause 5pA of current to flow, which is greater than the LM393/LM339's input bias current at +27°C (±6pA, typical). It is recommended to use multi-layer PCB layout and route the comparator's -IN and +IN signal under the PCB surface.

The effective way to reduce surface leakage is to use a guard ring around sensitive pins (or traces). The guard ring is biased at the same voltage as the sensitive pin. An example of this type of layout is shown in Figure 5 for Inverting configuration application.

1. For Non-Inverting Configuration:
   a) Connect the non-inverting pin (V_{IN}+) to the input with a wire that does not touch the PCB surface.
   b) Connect the guard ring to the inverting input pin (V_{IN}–). This biases the guard ring to the same reference as the comparator.
2. For Inverting Configuration:
   a) Connect the guard ring to the non-inverting input pin (V_{IN}+). This biases the guard ring to the same reference voltage as the comparator (e.g., V_{DD}/2 or ground).
   b) Connect the inverting pin (V_{IN}–) to the input with a wire that does not touch the PCB surface.

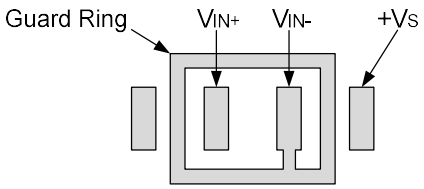


Figure 5. Example Guard Ring Layout for Inverting Comparator

Ground Sensing and Rail to Rail Output

The LM393/339 family implements a rail-to-rail topology that is capable of swinging to within 10mV of either rail. Since the inputs can go 300mV beyond either rail, the comparator can easily perform 'true ground' sensing.

The maximum output current is a function of total supply voltage. As the supply voltage of the comparator increases, the output current capability also increases. Attention must be paid to keep the junction temperature of the IC below 150°C when the output is in continuous short-circuit condition. The output of the amplifier has reverse-biased ESD diodes connected to each supply. The output should not be forced more than 0.5V beyond either supply, otherwise current will flow through these diodes.

ESD

The LM393/339 family has reverse-biased ESD protection diodes on all inputs and output. Input and output pins can not be biased more than 300mV beyond either supply rail.

Power Supply Layout and Bypass

The LM393/339 family's power supply pin should have a local bypass capacitor (i.e., 0.01μF to 0.1μF) within 2mm for good high frequency performance. It can also use a bulk capacitor (i.e., 1μF or larger) within 100mm to provide large, slow currents. This bulk capacitor can be shared with other analog parts.

Good ground layout improves performance by decreasing the amount of stray capacitance and noise at the comparator's inputs and outputs. To decrease stray capacitance, minimize PCB lengths and resistor leads, and place external components as close to the comparator' pins as possible.

Proper Board Layout

The LM393/339 family is a series of fast-switching, high-speed comparator and requires high-speed layout considerations. For best results, the following layout guidelines should be followed:

1. Use a printed circuit board (PCB) with a good, unbroken low-inductance ground plane.
2. Place a decoupling capacitor (0.1μF ceramic, surface-mount capacitor) as close as possible to supply.
3. On the inputs and the output, keep lead lengths as short as possible to avoid unwanted parasitic feedback around the comparator. Keep inputs away from the output.
4. Solder the device directly to the PCB rather than using a socket.
5. For slow-moving input signals, take care to prevent parasitic feedback. A small capacitor (1000 pF or less) placed between the inputs can help eliminate oscillations in the transition region. This capacitor causes some degradation to propagation delay when the impedance is low. The topside ground plane should be placed between the output and inputs.
6. The ground pin ground trace should run under the device up to the bypass capacitor, thus shielding the inputs from the outputs.

Typical Applications

IR Receiver

The LM393/339 is an ideal candidate to be used as an infrared receiver shown in Figure 6. The infrared photo diode creates a current relative to the amount of infrared light present. The current creates a voltage across R_D. When this voltage level cross the voltage applied by the voltage divider to the inverting input, the output transitions. Optional R_o provides additional hysteresis for noise immunity.

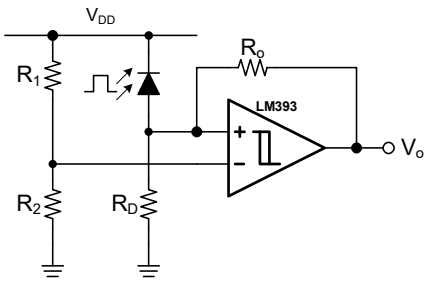


Figure 6. IR Receiver

Relaxation Oscillator

A relaxation oscillator using LM393/339 is shown in Figure 7. Resistors R_1 and R_2 set the bias point at the comparator's inverting input. The period of oscillator is set by the time constant of R_4 and C_1. The maximum frequency is limited by the large signal propagation delay of the comparator. LM393/339's low propagation delay guarantees the high frequency oscillation.

If the inverted input (V_{C1}) is lower than the non-inverting input (V_A), the output is high which charges C_1 through R_4 until V_{C1} is equal to V_A. The value of V_A at this point is

$$V_{A1} = \frac{V_{DD} \bullet R_2}{R_1 \parallel R_3 + R_2}$$

At this point the comparator switches pulling down the output to the negative rail. The value of V_A at this point is

$$V_{A2} = \frac{V_{DD} \bullet R_2 \parallel R_3}{R_1 + R_2 \parallel R_3}$$

If $R_1=R_2=R_3$, then $V_{A1}=2V_{DD}/3$, and $V_{A2}= V_{DD}/3$

The capacitor C_1 now discharges through R_4, and the voltage V_C decreases till it is equal to V_{A2}, at which point the comparator switches again, bringing it back to the initial stage. The time period is equal to twice the time it takes to discharge C_1 from $2V_{DD}/3$ to $V_{DD}/3$. Hence the frequency is:

$$Freq = \frac{1}{2 \bullet \ln 2 \bullet R_4 \bullet C_1}$$

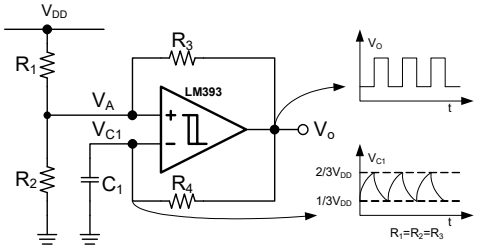


Figure 7. Relaxation Oscillator

Windowed Comparator

Figure 8 shows one approach to designing a windowed comparator using a single LM393/339 chip. Choose different thresholds by changing the values of R1, R2, and R3. OutA provides an active-low undervoltage indication, and OutB gives an active-low overvoltage indication. ANDing the two outputs provides an active-high, power-good signal. When input voltage V_i reaches the overvoltage threshold V_{OH}, the OutB gets low. Once V_i falls to the undervoltage threshold V_{UH}, the OutA gets low. When $V_{UH}<V_i<V_{OH}$, the AND Gate gets high.

$$V_{OH} = V_r \bullet (R_1 + R_2 + R_3)/R_1$$

$$V_{UH} = V_r \bullet (R_1 + R_2 + R_3)/(R_1 + R_2)$$

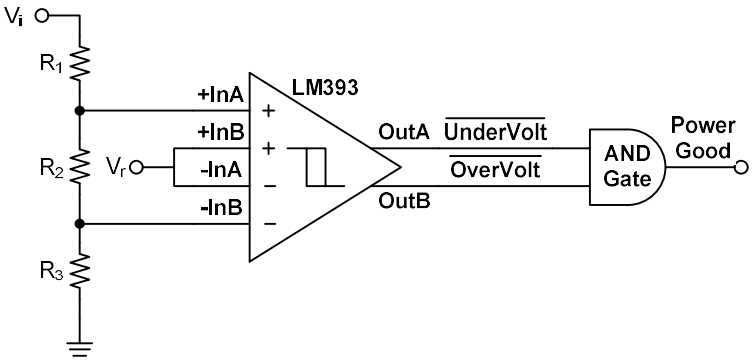
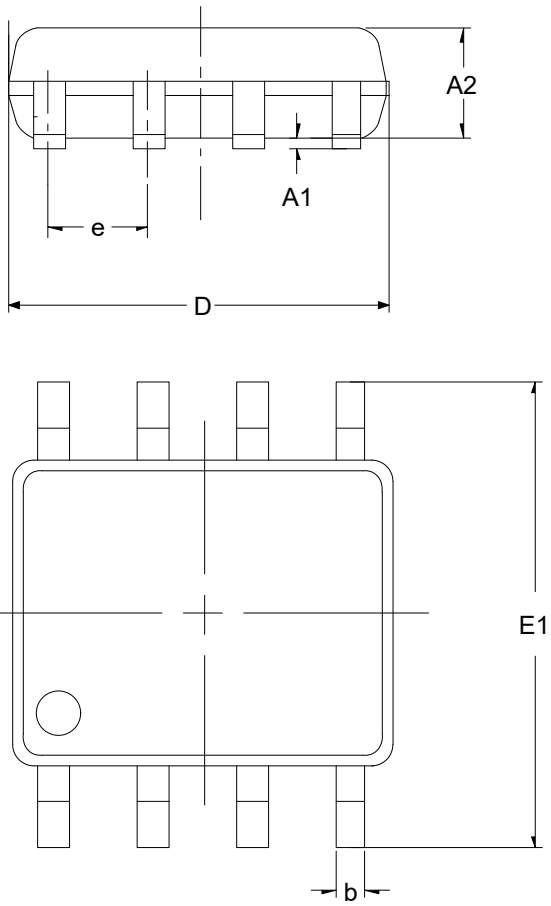


Figure 8. Windowed Comparator

Package Outline Dimensions

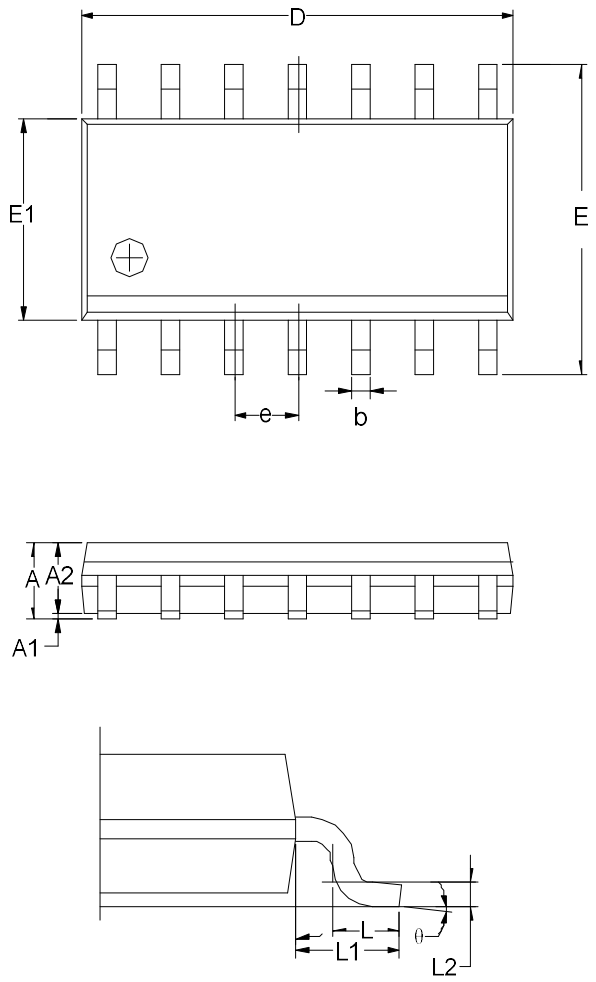
SO-8 (SOIC-8)



Symbol	Dimensions In Millimeters	
	Min	Max
A1	0.100	0.250
A2	1.300	1.550
b	0.330	0.510
C	0.170	0.250
D	4.780	5.000
E	3.800	4.000
E1	5.800	6.300
e	1.270TYP	
L1	0.400	0.900
θ	0°	8°

Package Outline Dimensions

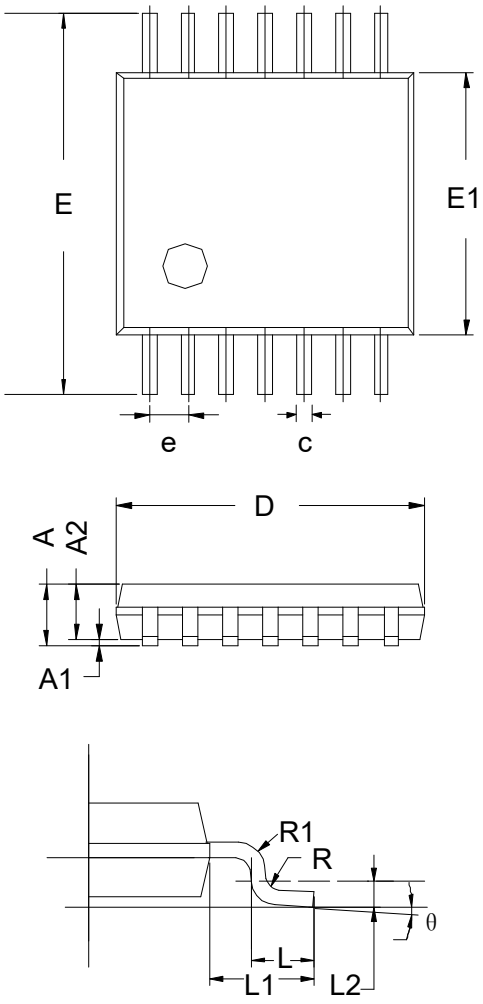
SO-14 (SOIC-14)



Symbol	Dimensions In Millimeters		
	MIN	TYP	MAX
A	1.35	1.60	1.75
A1	0.10	0.15	0.25
A2	1.25	1.45	1.65
b	0.31		0.51
D	8.45	8.63	8.85
E	5.80	6.00	6.20
E1	3.80	3.90	4.00
e	1.27 BSC		
L	0.40	0.60	0.80
L1	1.05 REF		
L2	0.25 BSC		
θ	0°		8°

Package Outline Dimensions

TSSOP-14



Symbol	Dimensions In Millimeters		
	MIN	TYP	MAX
A	-	-	1.20
A1	0.05	-	0.15
A2	0.80	-	1.05
c	0.19	-	0.30
D	4.86	5.00	5.10
E	6.20	6.40	6.60
E1	4.30	4.40	4.50
e	0.65 BSC		
L	0.45	0.60	0.75
L1	1.00 REF		
L2	0.25 BSC		
R	0.09	-	-
θ	0°	-	8°