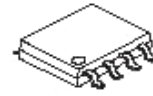
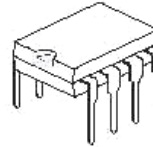


### DESCRIPTION

The JRC4558 is a high performance monolithic dual operational amplifier.



SOP-8

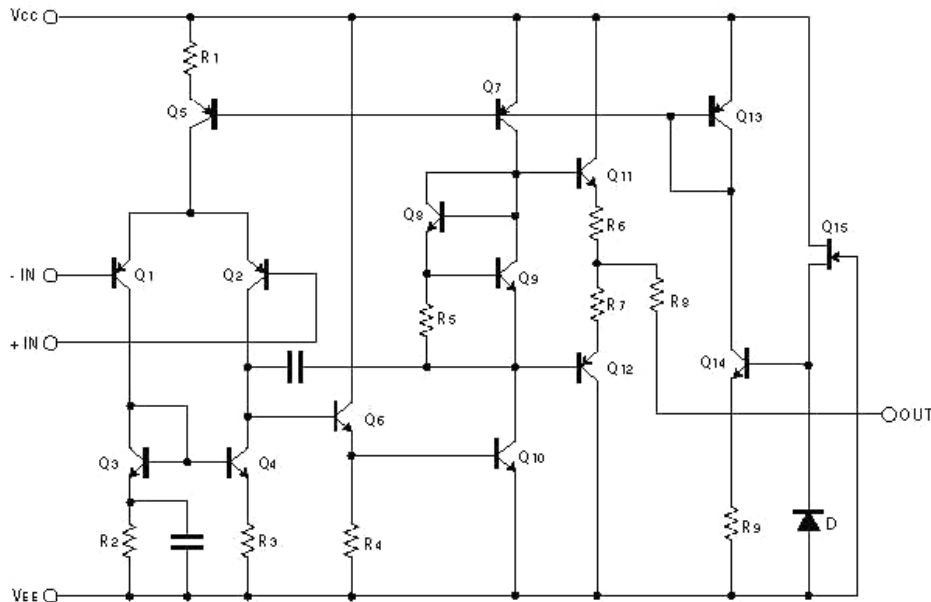


DIP-8

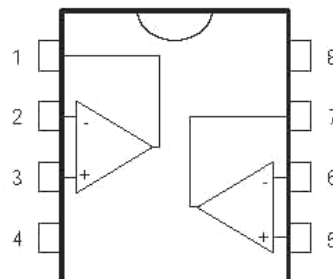
### FEATURES

- No frequency compensation required
- No latch – up
- Large common mode and differential voltage range
- Parameter tracking over temperature range
- Gain and phase match between amplifiers
- Internally frequency compensated
- Low noise input transistors
- Pin to pin compatible with MC1458/LM358

### BLOCK DIAGRAM (ONE SECTION ONLY)



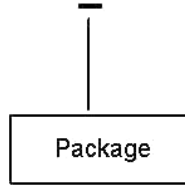
### PIN CONFIGURATION



- |                        |                         |
|------------------------|-------------------------|
| 1-Output 1             | 5-Non-inverting input 2 |
| 2-Inverting input 1    | 6-Inverting input 2     |
| 3-Non-inverting input1 | 7-Output 2              |
| 4-Vcc                  | 8-Vcc +                 |

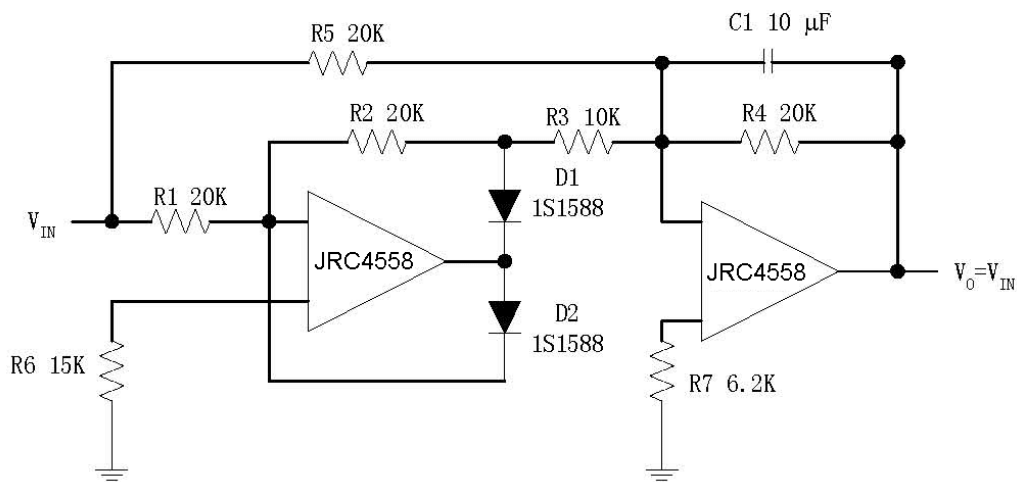
### ORDERING INFORMATION

JRC4558N



Blank SO-8  
N=PDIP8  
A=SO-8 & taping

### Typical Application



### MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage	V <sub>CC</sub>	±22	V
Differential Input Voltage	V <sub>I(DIFF)</sub>	±18	V
Input Voltage	V <sub>I</sub>	±15	V
Operating Temperature	TOPR	-20~ +85	
Power Dissipation P-DIP 8 SOP 8	PD	600 400	mW
Storage Temperature Range	TSTG	-65~+150	

### ELECTRICAL CHARACTERISTICS (V<sub>CC</sub>=15.0V, V<sub>EE</sub>=-15V, T<sub>A</sub>=25 °C, unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDUCTION	MIN	TYP	MAX	UNIT
Supply Current, all Amp, no load	I <sub>CC</sub>			2.3	4.5	mA
Input offset voltage	V <sub>IO</sub>	R <sub>s</sub> <10KΩ		2	6	mV
Input offset current	I <sub>IO</sub>			5	200	nA
Input bias current	I <sub>BIAS</sub>			30	500	nA
Large signal voltage gain	GV	V <sub>o(p-p)</sub> = ±10V, R <sub>L</sub> ≤2kΩ	20	200		V/mV
Common Mode Input Voltage Range	V <sub>I(R)</sub>		±12	±13		V

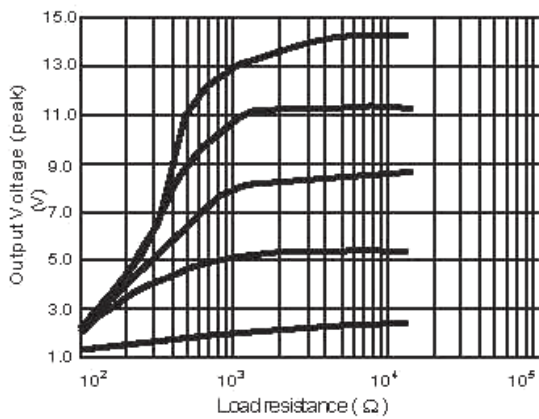
Common Mode Rejection Ratio	CMRR	$R_s \leq 10k\Omega$	70	90		dB
Supply Voltage Rejection Ratio	PSRR	$R_s \leq 10k\Omega$	76	90		dB
Output Voltage swing	$V_o(p-p)$	$R_L \geq 10k\Omega$		$\pm 12$	$\pm 14$	V
Power Consumption	$P_c$			70	170	mV
Slew Rate	SR	$V_i = \pm 10V, R_L \geq 2k\Omega, C_L \leq 100pF$	1.2	2.2		$V/\mu S$
Rise Time	$T_{RIS}$	$V_i = \pm 20mV, R_L \geq 2k\Omega, C_L \leq 100pF$		0.3		$\mu s$
Overshoot	OS	$V_i = \pm 20mV, R_L \geq 2k\Omega, C_L \leq 100pF$		15		%
Input Resistance	$R_i$		0.3	2		$M\Omega$
Output Resistance	$R_o$			75		$\Omega$
Total Harmonic Distortion	THD	$f=1KHz, A_v=20dB, R_L=2k\Omega, V_o=2V_{pp}, C_L=100pF$		0.008		%
Channel Separation	$V_{o1}/V_{o2}$			120		dB

### FREQUENCY CHARACTERISTICS ( $T_a=25^\circ C, V_{cc}=15V, V_{ee}=-15V$ )

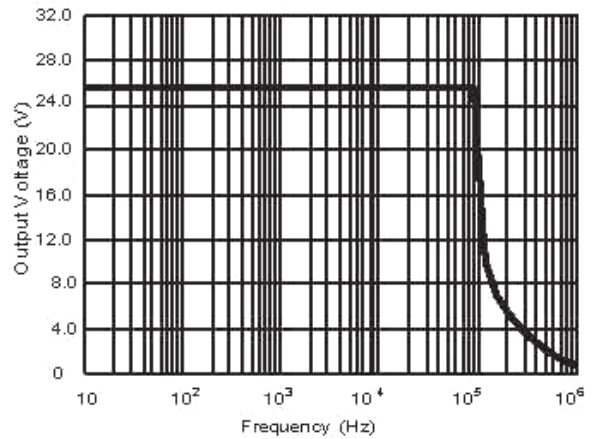
PARAMETER	SYMBOL	TEST CONDUCTION	MIN	TYP	MAX	UNIT
Unity Gain Bandwidth	BW		2.0	2.8		MHz

### TYPICAL PERFORMANCE CHARACTERISTICS

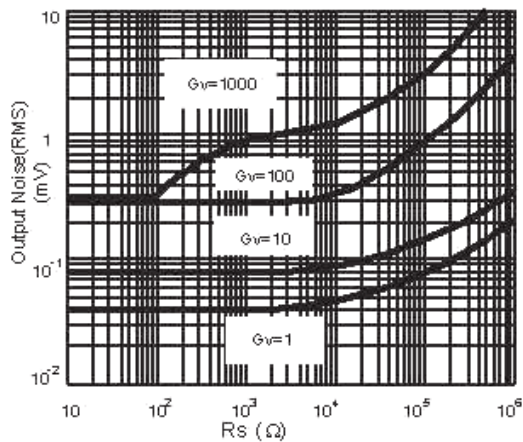
Positive output voltage swing vs load resistance



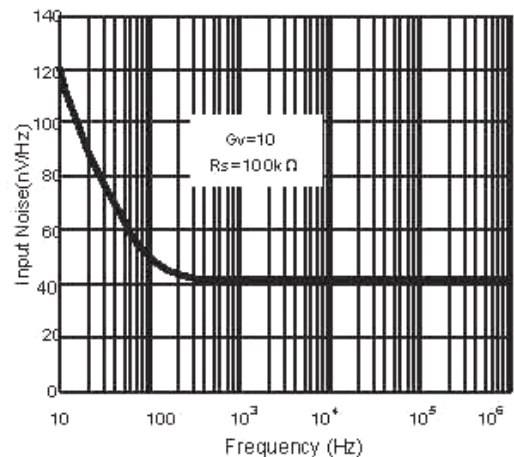
Power Bandwidth (Large Signal)



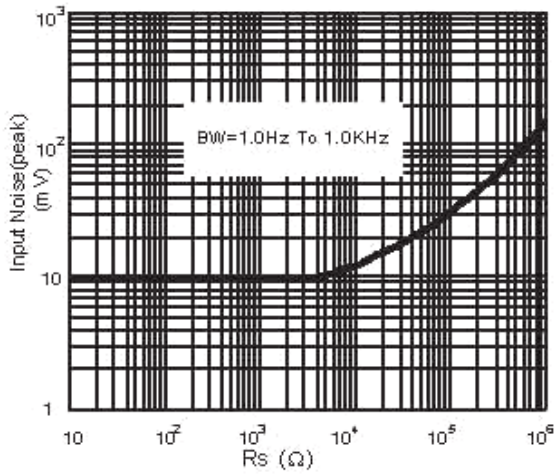
Output Noise vs  $R_s$



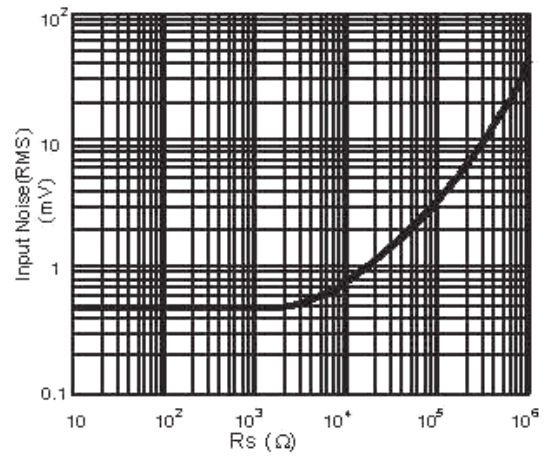
Spectral Noise Density



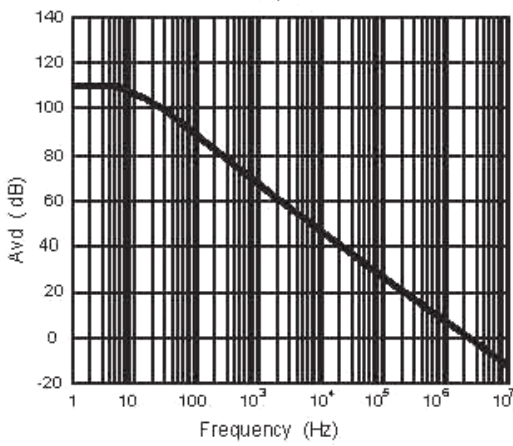
Burst Noise vs Rs



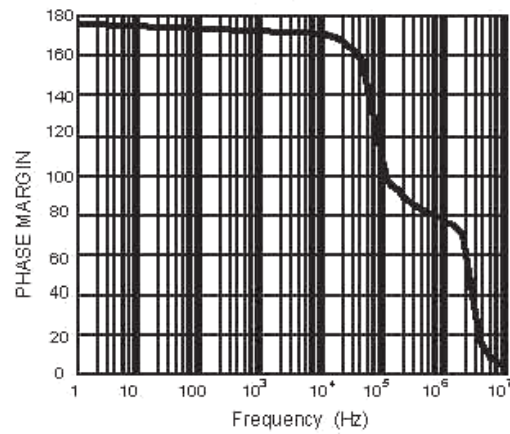
RMS Noise vs Rs



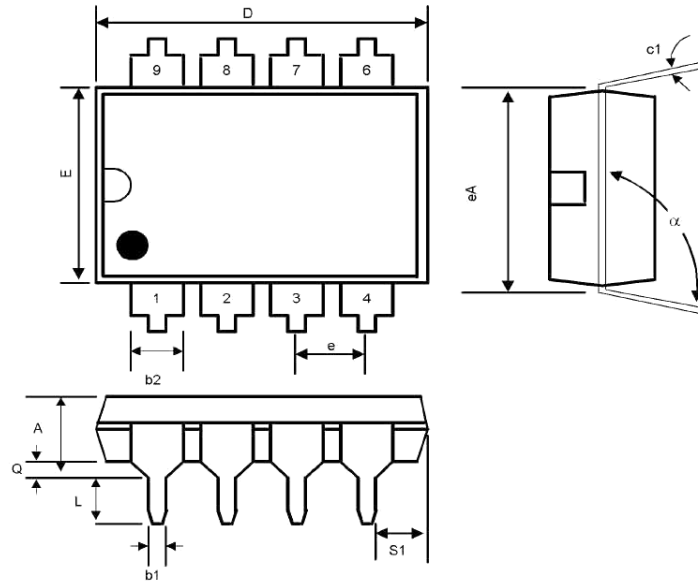
Open loop frequency response



PHASE MARGIN vs FREQUENCY

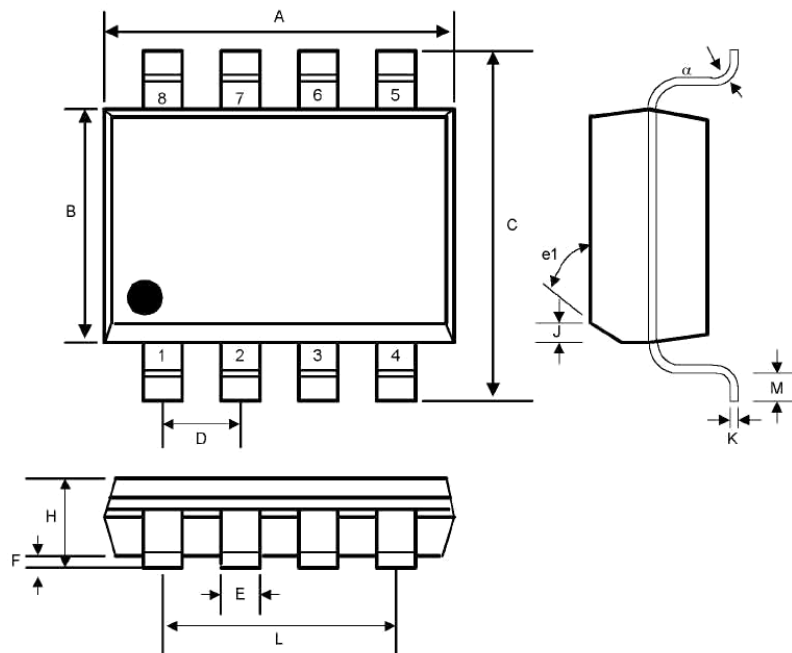


### Package Outlines: DIP-8



SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	-	0.200	-	5.08	-
b1	0.014	0.023	0.36	0.58	-
b2	0.045	0.065	1.14	1.65	-
c1	0.008	0.015	0.20	0.38	-
D	0.355	0.400	9.02	10.16	-
E	0.220	0.310	5.59	7.87	-
e	0.100 BSC		2.54 BSC		-
eA	0.300 BSC		7.62 BSC		-
L	0.125	0.200	3.18	5.08	-
Q	0.015	0.060	0.38	1.52	-
s1	0.005	-	0.13	-	-
α	90 <sup>0</sup>	105 <sup>0</sup>	90 <sup>0</sup>	105 <sup>0</sup>	-

### Small Outline SOP-8



SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.188	0.197	4.80	5.00	-
B	0.149	0.158	3.80	4.00	-
C	0.228	0.244	5.80	6.20	-
D	0.050	BSC	1.27	BSC	-
E	0.013	0.020	0.33	0.51	-
F	0.004	0.010	0.10	0.25	-
H	0.053	0.069	1.35	1.75	-
J	0.011	0.019	0.28	0.48	-
K	0.007	0.010	0.19	0.25	-
M	0.016	0.050	0.40	1.27	-
L	0.150	REF	3.81	REF	-
e1	45 <sup>0</sup>		45 <sup>0</sup>		-
α	0 <sup>0</sup>	8 <sup>0</sup>	0 <sup>0</sup>	8 <sup>0</sup>	-

\*All specs and applications shown above subject to change without prior notice.