

N-Channel Power MOSFET (50A, 60Volts)

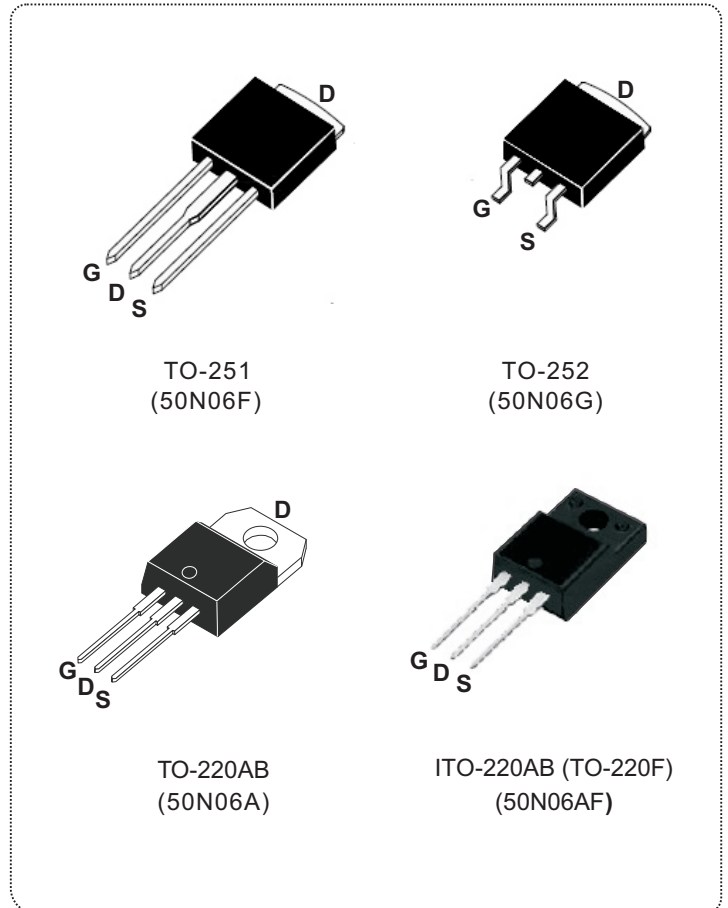
DESCRIPTION

The Nell **50N06** is a three-terminal silicon device with current conduction capability of 50A, fast switching speed, low on-state resistance, breakdown voltage rating of 60V, and max. threshold voltage of 4 volts.

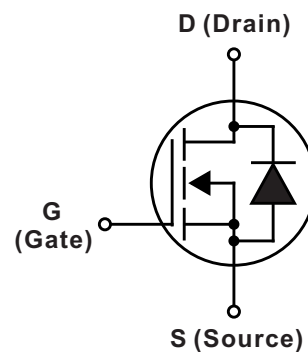
They are designed for use in applications such as switching regulators, switching converters, motor drivers and relay drivers. These transistors can be operated directly from integrated circuits.

FEATURES

- $R_{DS(ON)} = 22m\Omega @ V_{GS} = 10V$
- Ultra low gate charge(40nC max.)
- Low reverse transfer capacitance ($C_{RSS} = 80pF$ typical)
- Fast switching capability
- 100% avalanche energy specified
- Improved dv/dt capability
- 175°C operation temperature



PRODUCT SUMMARY	
I_D (A)	50
V_{DSS} (V)	60
$R_{DS(ON)}$ (Ω)	0.022 @ $V_{GS} = 10V$
Q_G (nC) max.	40

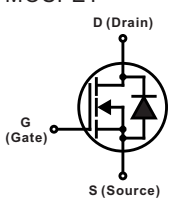


ABSOLUTE MAXIMUM RATINGS ($T_C = 25^\circ\text{C}$ unless otherwise specified)				
SYMBOL	PARAMETER	TEST CONDITIONS	VALUE	UNIT
V_{DSS}	Drain to Source voltag	$T_J=25^\circ\text{C}$ to 150°C	60	V
V_{DGR}	Drain to Gate voltage	$R_{GS}=20\text{K}\Omega$	60	
V_{GS}	Gate to Source voltage		± 20	
I_D	Continous Drain Current	$T_C=25^\circ\text{C}$	50	A
		$T_C=100^\circ\text{C}$	35	
I_{DM}	Pulsed Drain current(Note 1)		200	
E_{AS}	Single pulses avalanche energy(Note 2)		480	mJ
E_{AR}	Repetitive avalanche energy(Note 1)		13	
dv/dt	Peak diode recovery dv/dt(Note 3)		7	V/ns
P_D	Total power dissipation, $T_C=25^\circ\text{C}$	TO-251	130	W
		TO-252	130	
		TO-220	120	
		TO-220F	70	
T_J	Operation junction temperature		-55 to 175	$^\circ\text{C}$
T_{STG}	Storage temperature		-55 to 175	
T_L	Maximum soldering temperature, for 10 seconds	1.6mm from case	300	
	Mounting torque, #6-32 or M3 screw		10 (1.1)	lbf·in (N·m)

Note: 1.Repetitive rating: pulse width limited by junction temperature.
 2.L = 5.6mH, $I_{AS} = 50\text{A}$, $V_{DD} = 25\text{V}$, $R_G = 0\Omega$, starting $T_J=25^\circ\text{C}$.
 3. $I_{SD} \leq 50\text{A}$, $di/dt \leq 300\text{A}/\mu\text{s}$, $V_{DD} \leq V_{(BR)DSS}$, starting $T_J=25^\circ\text{C}$.

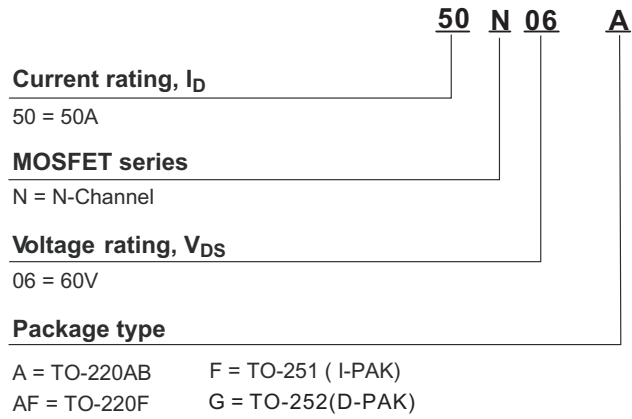
THERMAL RESISTANCE					
SYMBOL	PARAMETER	Min.	Typ.	Max.	UNIT
$R_{th(j-c)}$	Thermal resistance, junction to case	TO-251/TO-252		1.15	$^\circ\text{C}/\text{W}$
		TO-220		1.24	
		TO-220F		1.78	
$R_{th(c-s)}$	Thermal resistance, case to heatsink		0.5		
$R_{th(j-a)}$	Thermal resistance, junction to ambient	TO-251/TO-252		100	
		TO-220/TO-220F		62.5	

ELECTRICAL CHARACTERISTICS (T _C = 25°C unless otherwise specified)						
SYMBOL	PARAMETER	TEST CONDITIONS	Min.	Typ.	Max.	UNIT
V _{(BR)DSS}	Drain to source breakdown voltage	I _D = 250μA, V _{GS} = 0V	60			V
ΔV _{(BR)DSS} /ΔT _J	Breakdown voltage temperature coefficient	I _D = 250μA, referenced to 25°C		0.07		V/°C
I _{DSS}	Drain to source leakage current	V _{DS} = 60V, V _{GS} = 0V	T _C = 25°C		1.0	μA
			T _C = 150°C		50	
I _{GSS}	Gate to source forward leakage current	V _{GS} = 20V, V _{DS} = 0V			100	nA
	Gate to source reverse leakage current	V _{GS} = -20V, V _{DS} = 0V			-100	
R _{DS(ON)}	Static drain to source on-state resistance	I _D = 50A, V _{GS} = 10V		18	22	mΩ
V _{GS(TH)}	Gate threshold voltage	V _{GS} = V _{DS} , I _D = 250μA	2.0		4.0	V
C _{ISS}	Input capacitance	V _{DS} = 25V, V _{GS} = 0V, f = 1MHz		900	1220	pF
C _{OSS}	Output capacitance			430	550	
C _{RSS}	Reverse transfer capacitance			80	100	
t _{d(ON)}	Turn-on delay time	V _{DD} = 30V, I _D = 25A, R _G = 50Ω (Note 1, 2)		40	60	ns
t _r	Rise time			100	200	
t _{d(OFF)}	Turn-off delay time			90	180	
t _f	Fall time			80	160	
Q _G	Total gate charge	V _{DS} = 48V, V _{GS} = 10V, I _D = 50A (Note 1, 2)		30	40	nC
Q _{GS}	Gate to source charge			9.6		
Q _{GD}	Gate to drain charge (Miller charge)			10		

SOURCE TO DRAIN DIODE RATINGS AND CHARACTERISTICS (T _C = 25°C unless otherwise specified)						
SYMBOL	PARAMETER	TEST CONDITIONS	Min.	Typ.	Max.	UNIT
V _{SD}	Diode forward voltage	I _{SD} = 50A, V _{GS} = 0V			1.5	V
I _S	Continuous source current	Integral reverse P-N junction diode in the MOSFET 			50	A
I _{SM}	Pulsed source current				200	
t _{rr}	Reverse recovery time	I _S = 50A, V _{GS} = 0V, dI _F /dt = 100A/μs		55		ns
Q _{rr}	Reverse recovery charge				80	

Note: 1. Pulse test: Pulse width ≤ 300μs, duty cycle ≤ 2%.
2. Essentially independent of operating temperature.

ORDERING INFORMATION SCHEME



■ TEST CIRCUITS AND WAVEFORMS

Fig.1A Peak diode recovery dv/dt test circuit

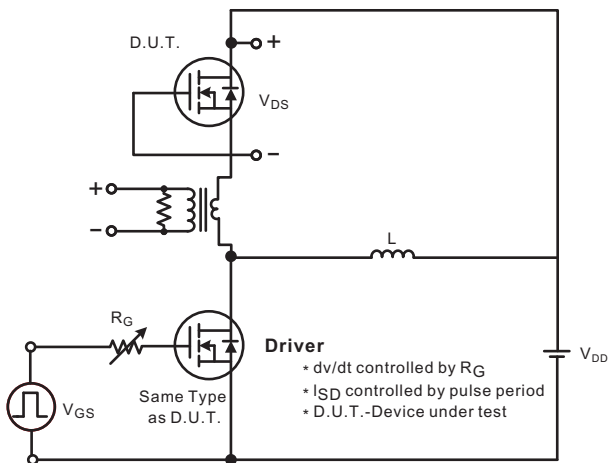
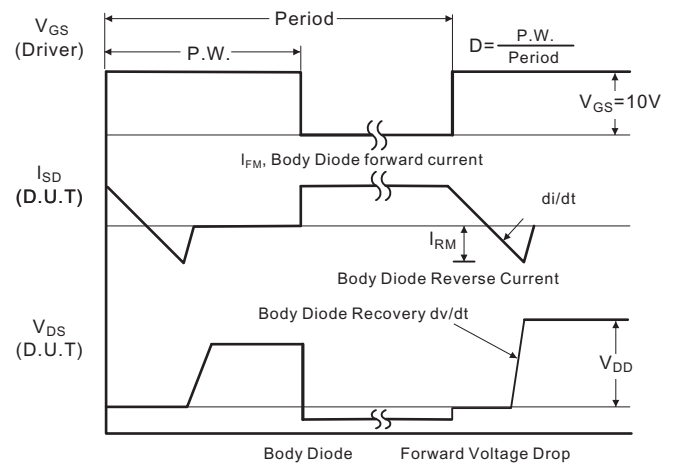


Fig.1B Peak diode recovery dv/dt waveforms



■ TEST CIRCUITS AND WAVEFORMS (Cont.)

Fig.2A Switching test circuit

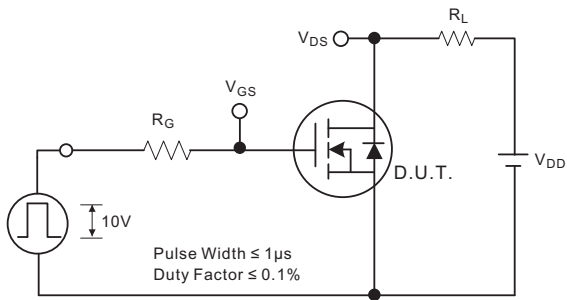


Fig.2B Switching Waveforms

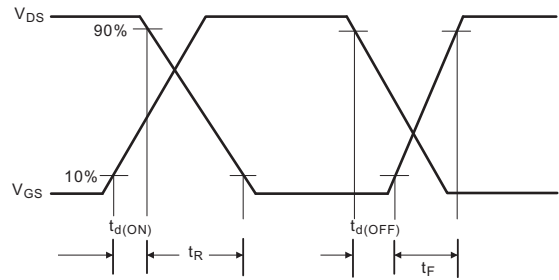


Fig.3A Gate charge test circuit

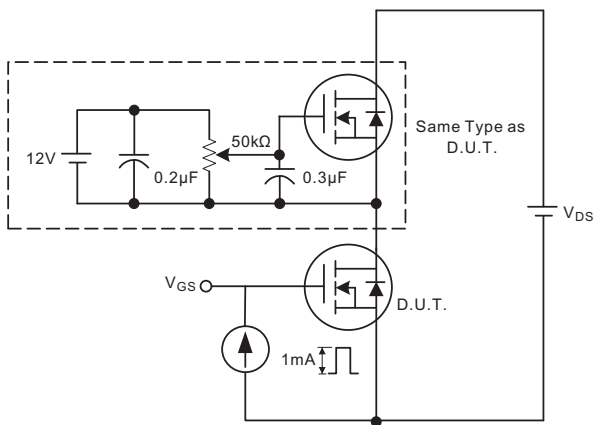


Fig.3B Gate charge waveform

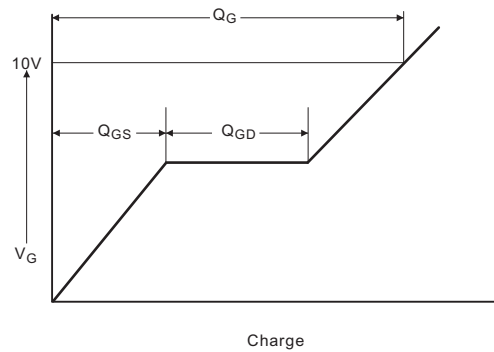


Fig.4A Unclamped Inductive switching test circuit

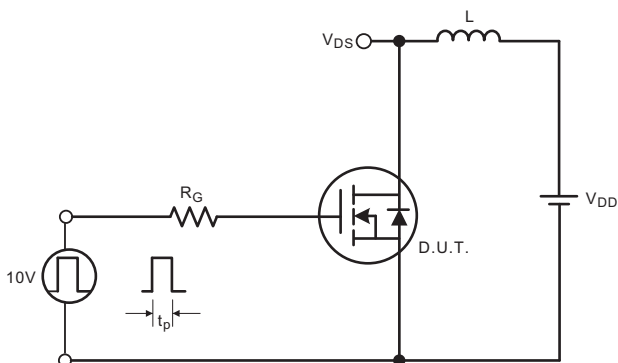
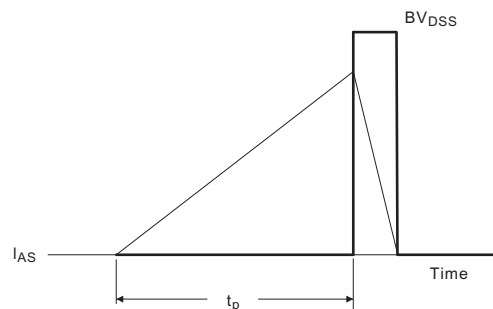


Fig.4B Unclamped Inductive switching waveforms



TYPICAL CHARACTERISTICS

Fig.1 On-State characteristics

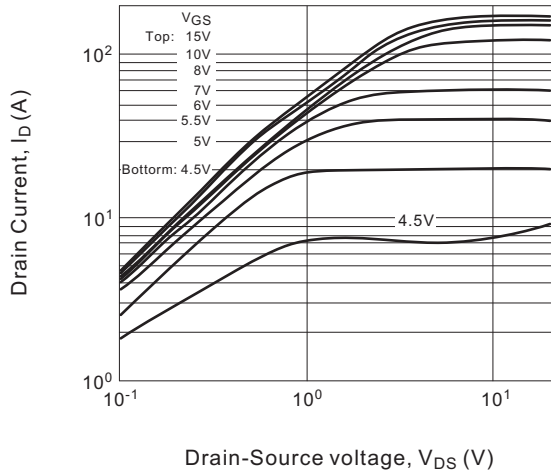


Fig.2 Transfer characteristics

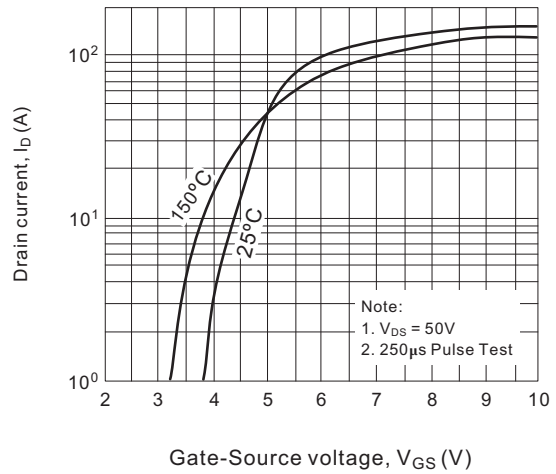


Fig.3 On-Resistance variation vs drain current and gate voltage

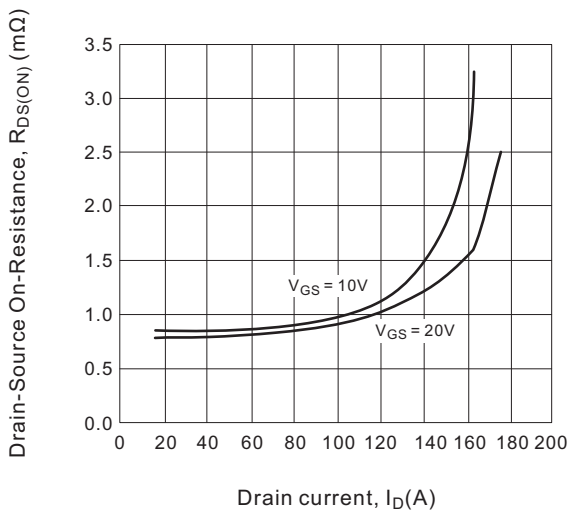


Fig.4 On state current vs. allowable case temperature

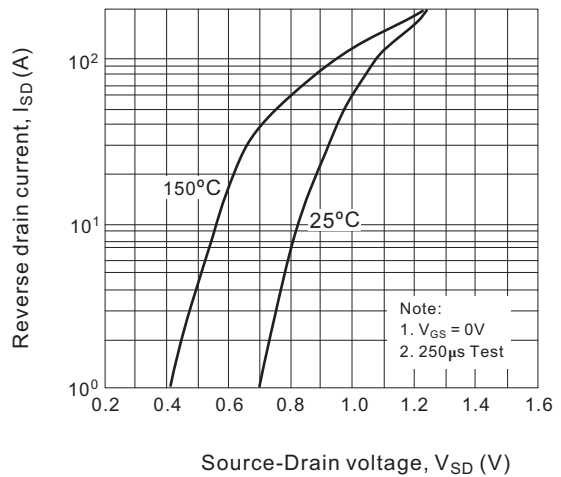


Fig.5 Capacitance characteristics (Non-Repetitive)

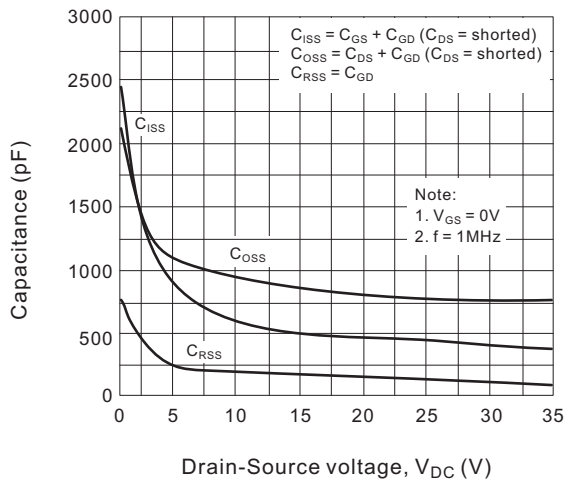


Fig.6 Gate charge characteristics

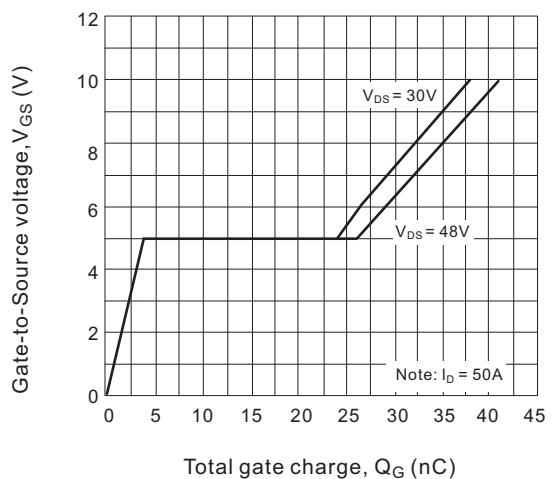


Fig.7 Breakdown voltage variation vs junction temperature

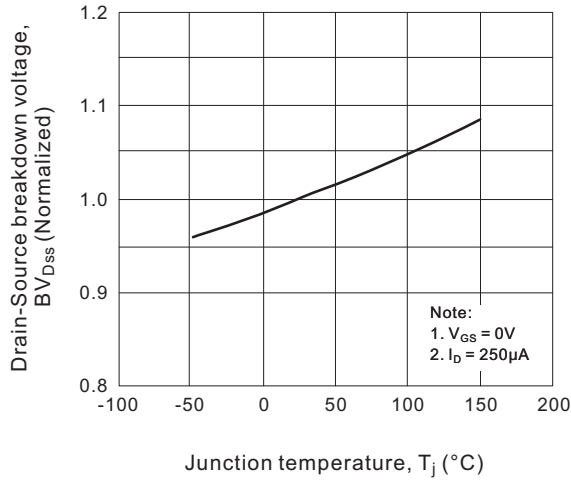


Fig.8 On-Resistance variation vs junction temperature

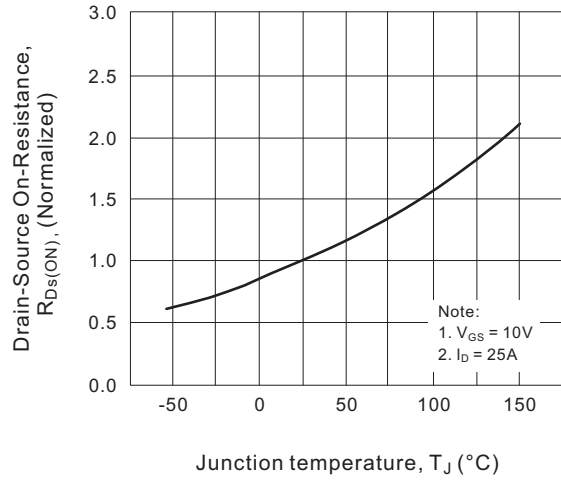


Fig.9 Maximum safe operating

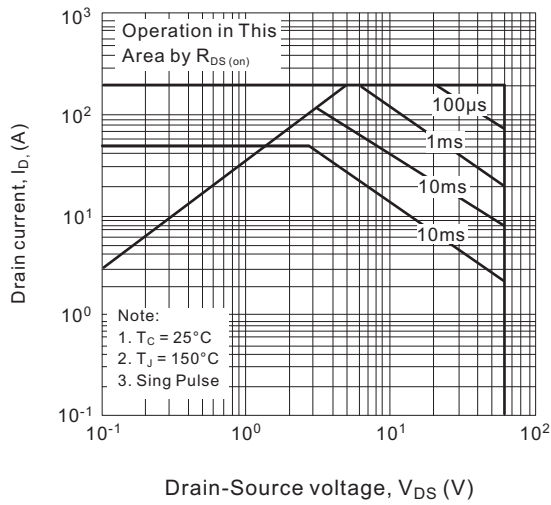


Fig.10 Maximum drain current vs. case temperature

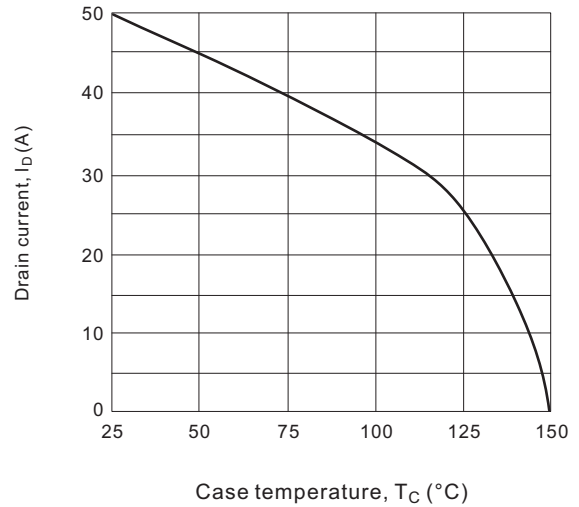
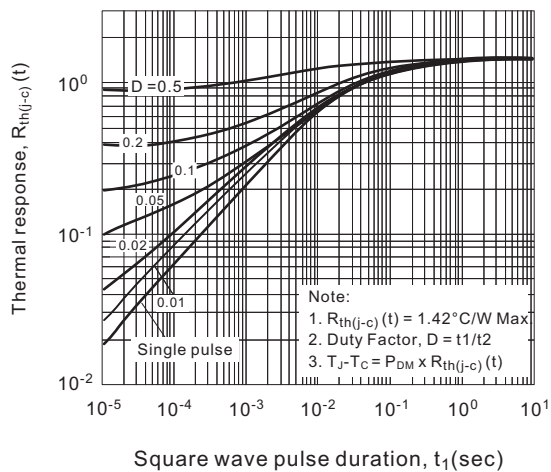


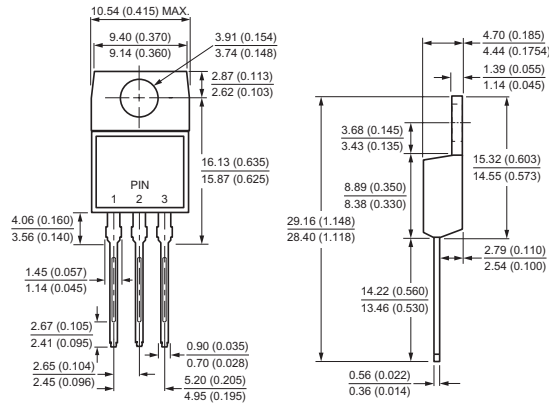
Fig.11 Transient thermal response curve



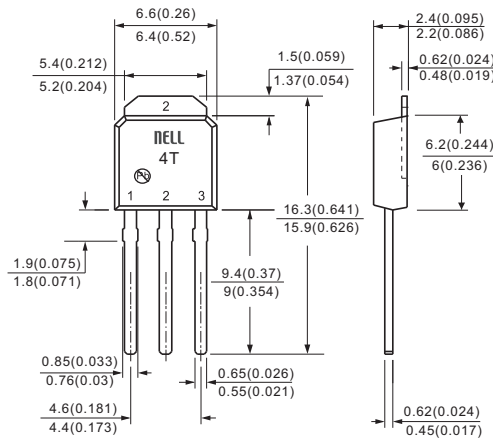
Case Style

Nell High Power Products

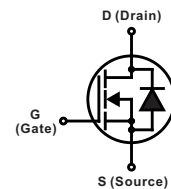
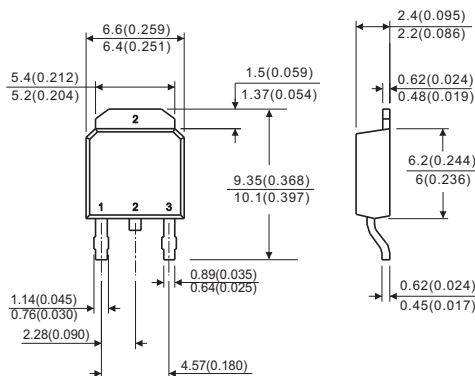
TO-220AB



TO-251 (I-PAK)



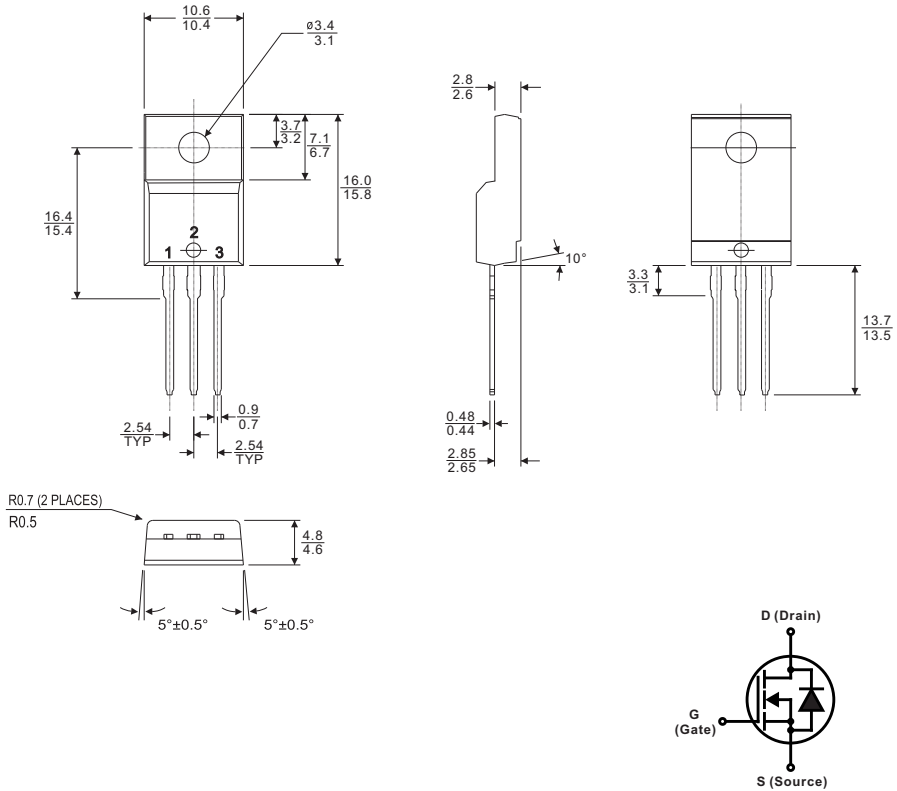
TO-252 (D-PAK)



All dimensions in millimeters(inches)

Case Style

ITO-220AB



All dimensions in millimeters